TR-808 SERVICE NOTES

First Edition

Second Printing (July 12, 1983 E2)

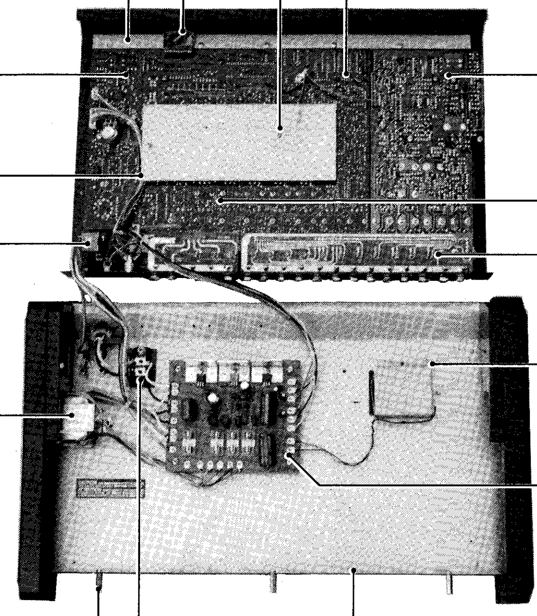
SPECIFICATIONS

Rhythm storage capacity	1-32 steps/measure 64 measures x 12 tracks
Tempo variable range	4M = 40-300
Master output	Hi 6V p-p/1KΩ; Lo 0.6V p-p/3KΩ (Level: Voices @ red mark; AC @ FCW)
Multi output	1KΩ
Trigger output	+15V, 20ms; 1KΩ —CB/CP(MA)/AC—
Accent level	0dB-10dB
Power consumption	8W
Dimensions	508 (w) x 305 (d) x 110 (h) mm
Net weight	5kg

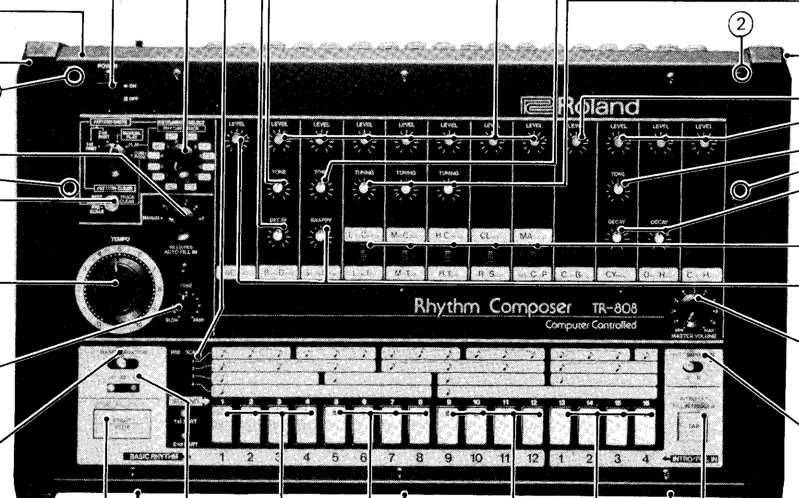
CAUTION

Although some parts are designated in abridged number or numberless in this limited space, they are fully numbered on the Parts List.

Parts order must be written in full number followed by the part name to encourage prompt, accurate dispatch.



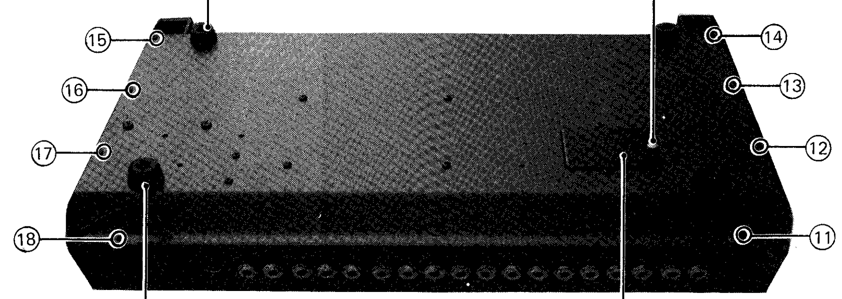
TOP PANEL REMOVAL SCREWS: ①– ⑩



① – ④ 3 x 10 mm B1, Fe, Br, Biding, Self tapping

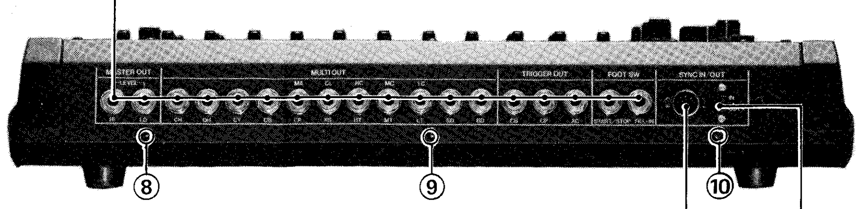
⑤ – ⑦ 3 x 6 mm Fe, Br Binding

TOP PANEL REMOVAL SCREWS
1 through 10

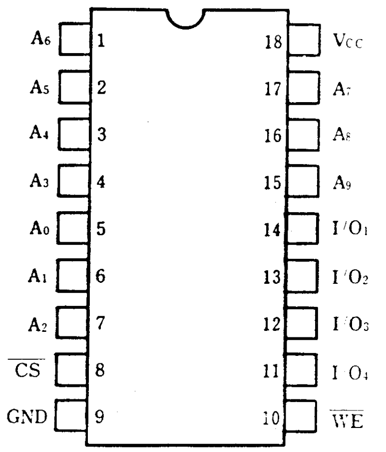


SCREWS ⑧ – ⑩ 3 x 6 mm B1, Fe, Br Binding, Self tapping

SCREWS ⑪ – ⑱ 3 x 10 mm B1, Fe, Br Binding, Self tapping

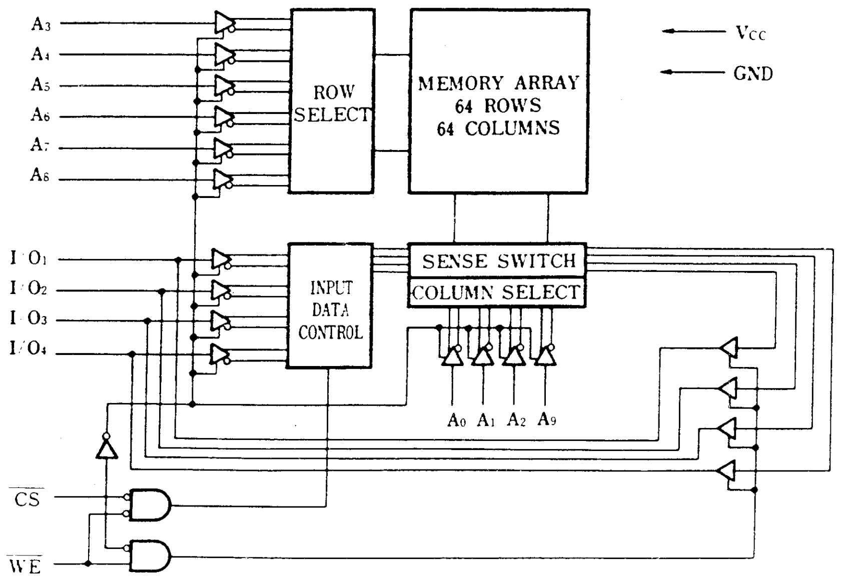


(Top View)



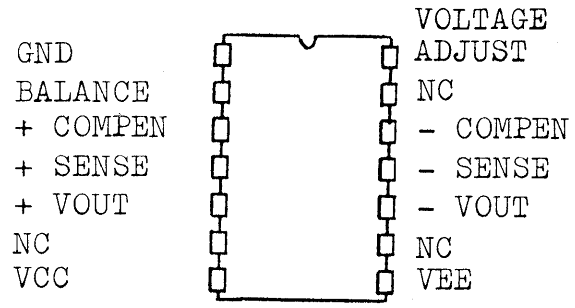
μPD444C
HM4334P-4

1024-word×4-bit Static CMOS RAM

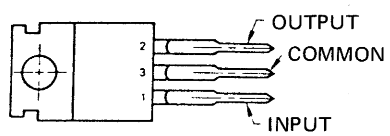


TA7179P

DUAL ±15V TRACKING RAGULATOR



Reg.IN = 5mV(typ)(VIN=18-30V)
Reg.OUT= 5mV(typ)(IOUT=0-50mA)
Ripple rejection ratio = 75dB
Output current = 100mA (max)



μA7800 SERIES

3-TERMINAL POSITIVE VOLTAGE REGULATORS

ORDER INFORMATION

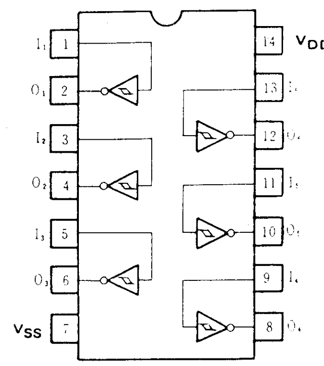
OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA7805C	μA7805UC
6 V	μA7806C	μA7806UC
8 V	μA7808C	μA7808UC
8.5 V	μA7885C	μA7885UC
12 V	μA7812C	μA7812UC
15 V	μA7815C	μA7815UC
18 V	μA7818C	μA7818UC
24 V	μA7824C	μA7824UC

ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)		35 V
(24 V)		40 V
Internal Power Dissipation		Internally Limited
Storage Temperature Range		−65°C to +150°C
Operating Junction Temperature Range	μA7800	−55°C to +150°C
	μA7800C	0°C to +150°C
Lead Temperature (Soldering, 60 s time limit) TO-3 Package		300°C
(Soldering, 10 s time limit) TO-220 Package		230°C

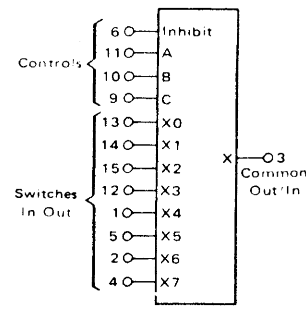
HD14584B

Hex Schmitt Trigger



MC14051B

8-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

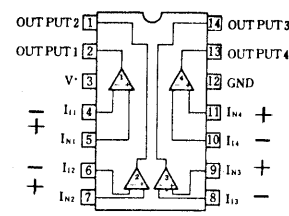
TRUTH TABLE

Control Inputs				ON Switches		
	Select					
Inhibit	C*	B	A	MC14051B	MC14052B	MC14053B
0	0	0	0	X0	Y0 X0	Z0 Y0 X0
0	0	0	1	X1	Y1 X1	Z0 Y0 X1
0	0	1	0	X2	Y2 X2	Z0 Y1 X0
0	0	1	1	X3	Y3 X3	Z0 Y1 X1
0	1	0	0	X4		Z1 Y0 X0
0	1	0	1	X5		Z1 Y0 X1
0	1	1	0	X6		Z1 Y1 X0
0	1	1	1	X7		Z1 Y1 X1
1	x	x	x	None	None	None

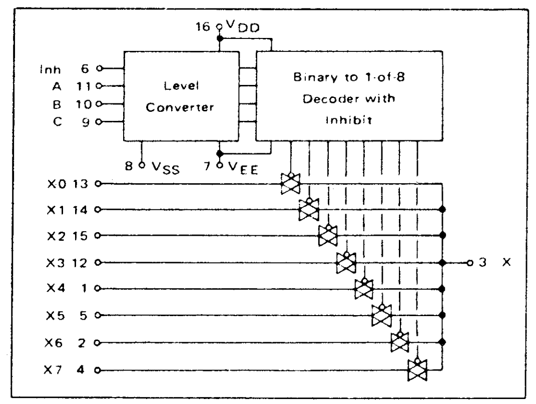
*Not applicable for MC14052
x = Don't Care

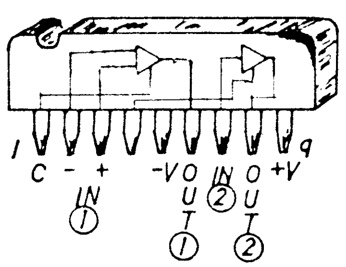
AN6912

Quad Comparator

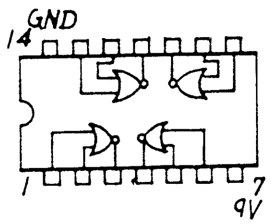


MC14051B FUNCTIONAL DIAGRAM





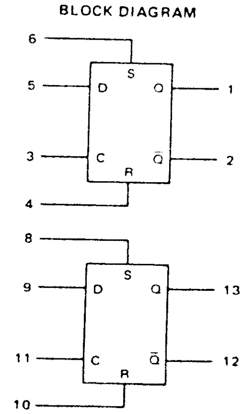
BA662



MC14001B CP

Quad 2-Input NOR Gate

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

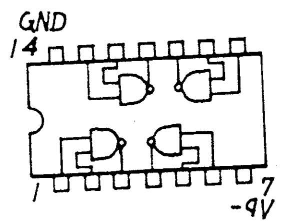
MC14013B

DUAL TYPE D FLIP-FLOP

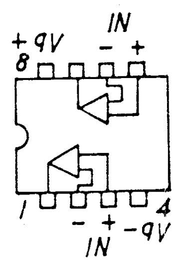
TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\bar{Q}$	
_/‾	0	0	0	0	1	
_/‾	1	0	0	1	0	
‾_	X	0	0	Q	$\bar{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

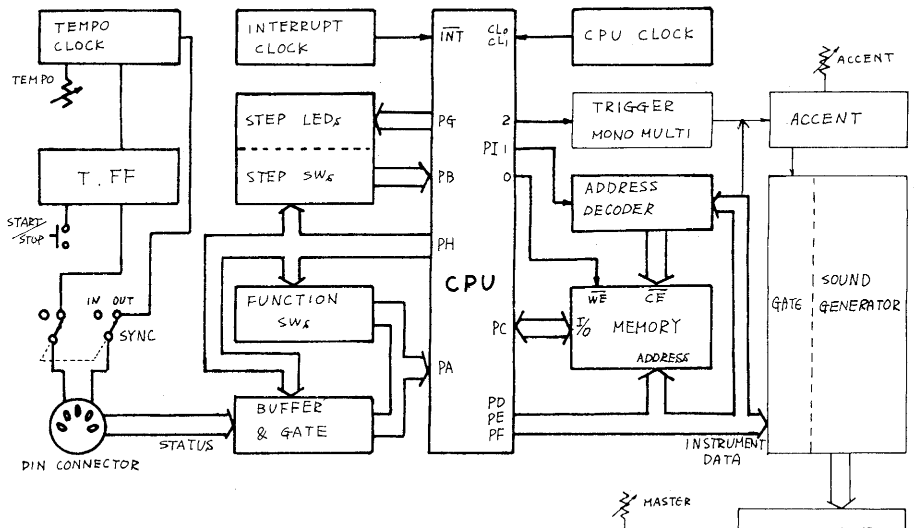


TC4011BP
Quad 2-Input NAND Gate



μPC 4558 C

TR-808 CIRCUIT DESCRIPTION



Thick line indicates
CPU controlled circuits,
thin line Voicing.

FIGURE 1 BLOCK DIAGRAM

μPD650C–085 FUNCTIONAL DESCRIPTION

Port	Bit	No.	Function		Code	Instrument data
PH (Port H)	0	26				
	1	27	Scanning signal outputs to switches			
	2	28	Switching signal outputs to STATUS BUFFER & GATE			
	3	29				
PA (Port A)	0	33				
	1	34	Switch scanning signal inputs			
	2	35	STATUS (TEMPO. CLOCK. START/STOP. FILL IN) inputs			
	3	36				
PB (Port B)	0	37	Inputs from STEP Switches (RHYTHM SELECT Swtiches)			
	1	38				
	2	39				
	3	40				
PG (Port G)	0	22	Drive signals to STEP LEDs			
	1	23				
	2	24				
	3	25				
PE (Port E)	0	12	1st/2nd		CP	
	1	13	A/B		RS	
	2	14	Memory bank		HT	
	3	15	select		MT	
PD (Port D)	0	8		MEMORY ADDRESSES	CH	INSTRUMENT DATA
	1	9	Rhythm numbers	These pins use CE from ADDRESS Decoder to select cells in RAM to be accessed	OH	These data need COMMON TRIG to trigger Sound Generators being designated
	2	10			CY	
	3	11			CB	
PF (Port F)	0	16			LT	
	1	17	Step		SD	
	2	18	numbers		BD	
	3	19			AC	
PC (Port C)	0	2	Data Inputs/Outputs			
	1	3				
	2	4				
	3	5				
PI (Port I)	0	30	Memory WE			
	1	31	Memory CE (associated with PE-2, 3 at ADDRESS DECODER)			
	2	32	Trigger Pulse (INSTRUMENT) output			

General

As can be seen from the block diagram, most processes of TR-808 up to generation of pulses triggering sound generators are controlled by the computer. CPU pin functions are as shown at the lower left table.

Once power is turned on for TR-808, pulses are generated from PI-2 of CPU regardless of TR-808 function mode (Start/Stop) and of presence or absence of rhythm patterns. The time length between the pulses is equal to that of the shortest rhythm patterns. The pulse is transfered to TRIGGER MONO, then ACCENT from which it is applied in parallel to all the gates prestaged to Sound Generators; accordingly, called COMMON TRIGGER. On the other hand, instrument data designating sound to be outputted are independently supplied to the gates from corresponding exclusive ports (PD, PE and PF). Since Instrument data are time sharing the data buss with memory addresses, the data are aligned with Common Trigs in timing. When these two signals are applied, the gate ANDs the two signals and outputs a signal triggering the sound generator. Since the peak value of this trig signal is in proportion to that of the Common Trig pulses, when an accent data is outputted, the data can be used to change the amplitude of the Common Trig signal.

Panel control settings are read by interruption of CPU each time an interrupt signal is fed to the $\overline{\text{INT}}$ terminal. First, the **Buffer & gate** turns on by a signal from PH, and the status is read through PA. Then, some statuses of function switches are read through PA by a signal from one port of PH. At the same time, some statuses of a group of step switches are read through PB, and the step LED drive signal is outputted from PG as required. Statuses are read each time an $\overline{\text{INT}}$ signal is fed. However, statuses of the step and function switches are read every four times of $\overline{\text{INT}}$ signals.

Four CMOS RAMs (1K x 4-bit) are used for data storage. Chips are selected when the upper two bits of PE data decoded by IC5 are enabled by pulses from PI-1. Addresses of chip memory cells are designated by bits of PD, PE and PF. Data storage to addresses are possible when an L output from PI-0 is applied to $\overline{\text{WE}}$.

Detail

SW Scanning, Status Reading

Reading of statuses of the controls on the panel (step switches, function switches, tempo, etc.) starts when an interrupt signal is applied to $\overline{\text{INT}}$ terminal every 1.9ms. When the signal is applied to $\overline{\text{INT}}$ terminal, CPU starts interruption. The interruption period is approx. 600μs. During the first 150μs, PH0–PH3 become H, and the collector of AND gate Q18 becomes L. STATUS signals are ANDed with this L by IC3 and read through PA. After 150μs, only PH-0 becomes L. This signal is converted to H by Q23, and reaches PB and PA through the closed contacts of the Step switches (No. 1–No. 4), SW1a (Mode) and SW2 (Clear). When one of the four Step switches is closed, the corresponding STEP LED lighting signal is immediately fed from PG. Since the PG output is latched until the next INT signal is applied, the lighting period is approx. 1.8ms. This period b is approx. 450μs. The remaining period c is for processing of main program. When the next INT signal is applied, PH0–PH3 become H again, the statuses of the TEMPO CLOCK, START/STOP, TAP, etc. are read again. Then, only PH1 becomes L and the statuses of switches connected to the collector of Q24 are read. At the next INT signal, STATUS and PH2 become L. Next, PH3 becomes L. This change is repeated. In this way statuses are checked each time an INT signal is applied every 1.9ms so that the CPU can respond to the status change promptly. The statuses of other switches are read every four times of INT signals. This corresponds to one reading every 7.6ms.

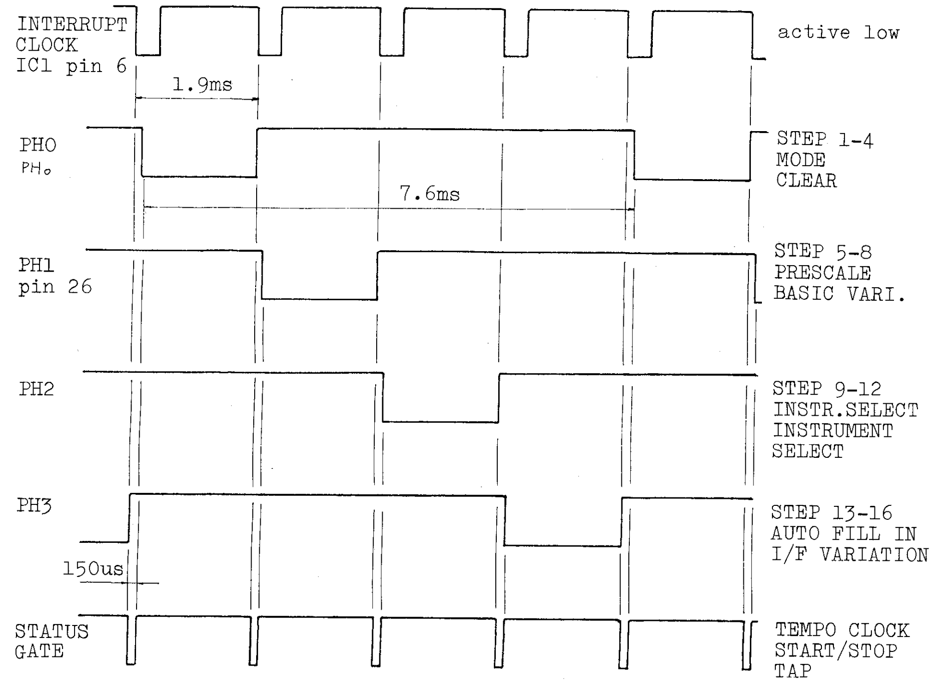
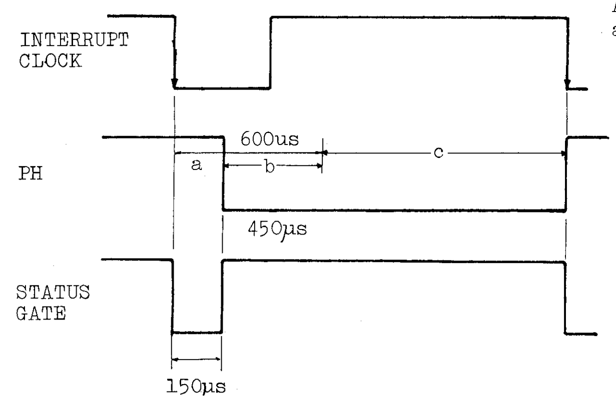


FIGURE 2
INTERRUPT CYCLE
TIMING DIAGRAM

All time lengths
are approximate.



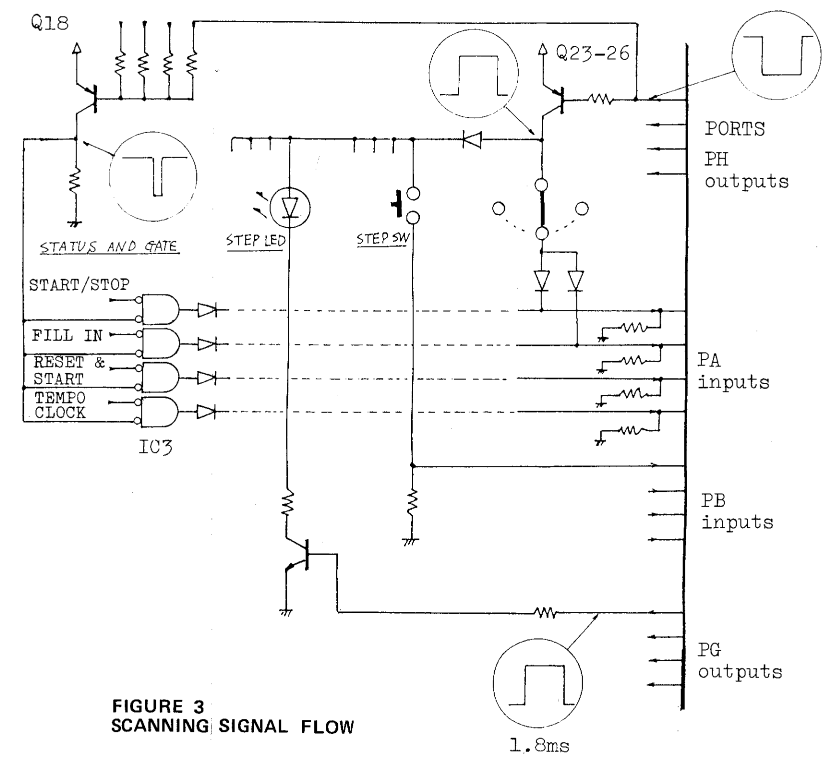


FIGURE 3
SCANNING SIGNAL FLOW

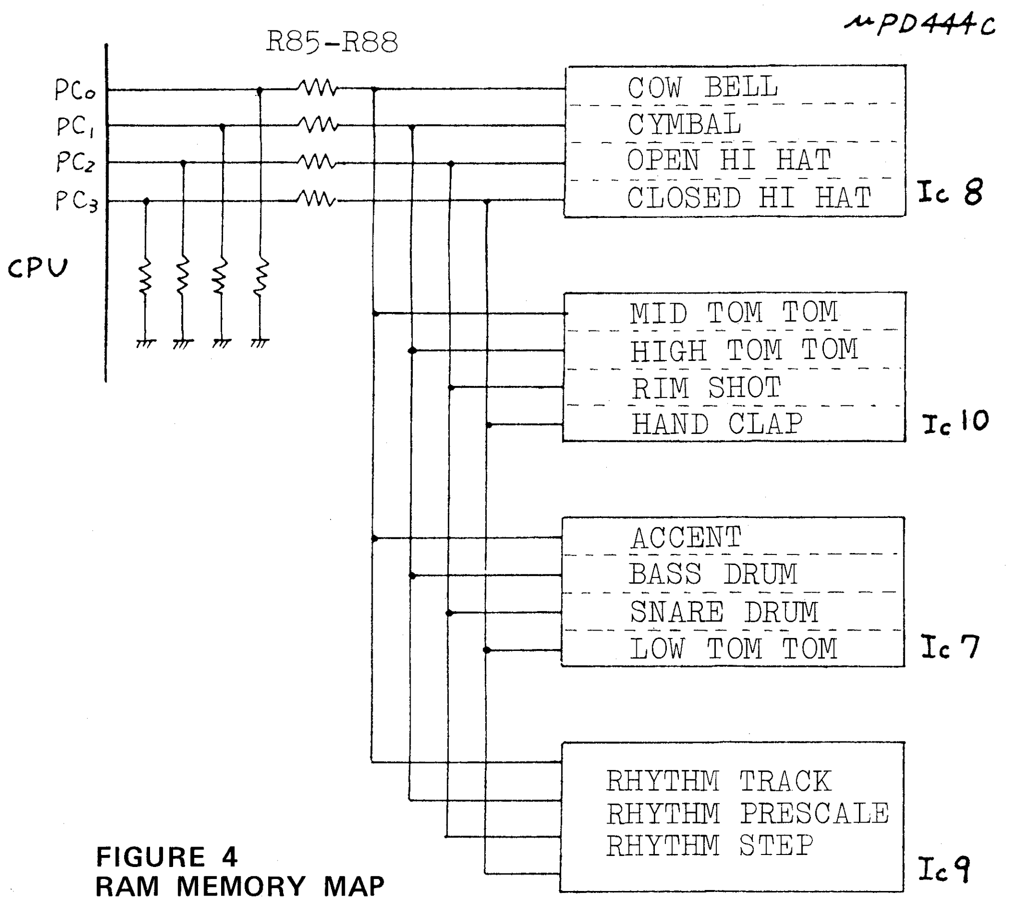


FIGURE 4
RAM MEMORY MAP

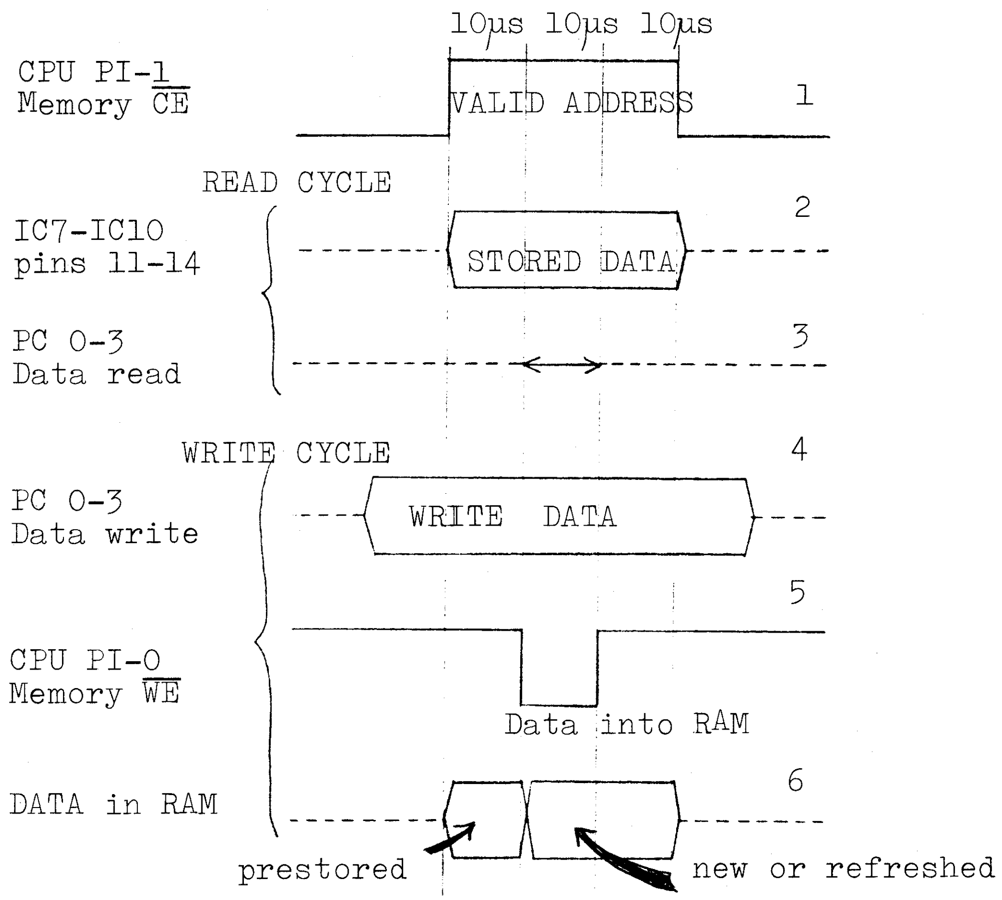


FIGURE 5 READ/WRITE CYCLE TIMING

RAM, Address Decoder

Four static CMOS RAMs (μPD444C, 1K x 4-bit) are used for memory. The memory map is shown in Fig. 4.

The upper two bits PE2 and PE3 of CPU designate a RAM, IC5 decodes these bits, and the memory select is enabled by a signal from PI-1 ($\overline{CE}$). See Fig. 5.

Cell addresses are designtated by bits from PD, PE and PF. After 10μs of $\overline{CE}$, the data shown in Fig. 5-2 is read (5-3) or a new data from PC is written (Fig. 5-5).

As can be seen from Fig. 5-2 and -4, during writing, PC output data and RAM data at the I/O ports of RAM may conflict with one another. To prevent this, the buffer resistors (R85—R88) are connected.

The LED driver transistors (Q2—Q5) for BASIC VARIATION, 1ST and 2ND are directly connected to the bus of PD and PE. However, since various data appear on the bus by time sharing processing, the LEDs may sometimes light even when unnecessary signals are applied, resulting in possible lighting timing disparity in a mode.

RAMs' low power consumption during high CE allows memories to be maintained for longer period with back-up battery.

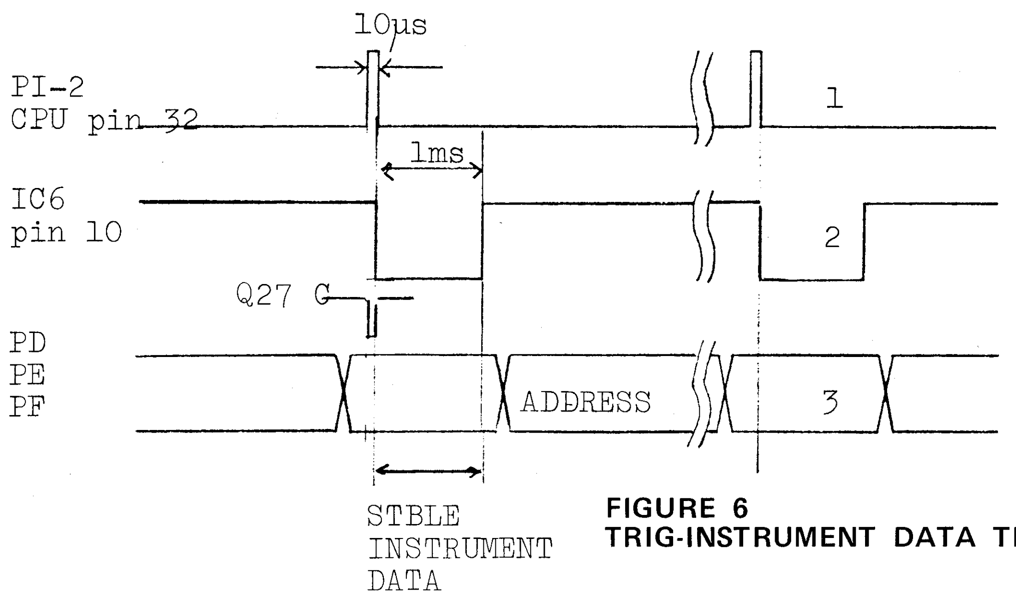


FIGURE 6
TRIG-INSTRUMENT DATA TIMING

Trigger Gate

Pulses corresponding to the shortest rhythm step usable by TR-808 are fed from PI-2 of CPU at a time interval determined by the setting of TEMPO CONTROL (Fig. 6-1). On the other hand, instrument data to be reproduced are applied from PD, PE and PF to the gate of each sound generator in synchronization with step pulses (Fig. 6-3). Since the step pulse width of 10μs is too narrow to trigger a sound generator, it is widened to approx. 1ms which is nearly equal to the width of instrument data signal. This widening is accomplished by the monostable IC6. It is triggered by a rising edge of Q27-inverted pulse. (Fig. 6-2). The L period is determined by the sum of the time constants of R100 x C23 and R102 x C27.

The output from pin 10 of IC6 passes through the ACCENT circuit composed of Q31—Q34, becomes a COMMON TRIG signal, and simultaneously applied to the gates of all sound generators in parallel. When instrument data is present at a gate, this trigger signal is ANDed with the data and activates the corresponding sound generator (See Fig. 7).

Since the AND output from the gate is in proportion to the amplitude of the common trig signal, the output of the sound generator has the amplitude in proportion to the common trig signal. Accordingly, when ACCENT data are present, they are added to the common trig signal. Since the output of pin 10 of IC6 is a negative logic signal, when there are no step pulses, the output signal becomes H, Q31 turns on and places a ground at base of Q32. When pin 10 of IC6 becomes L, Q31 becomes off, and when ACCENT data from PF-3 is L (no accent), Q34 turns on to shunt VR3. As a result, the base of Q32 becomes approx. +5V and trig amplitude is approx. 4V. When ACCENT data is H, a voltage between 5V and 15V according to VR3 setting is applied to the base of Q32, and is converted into trig pulses of approx. 4—14V. This explains that ACCENT level can be changed by VR3.

In the case of CB, CY, OH and CH, trig variation range is narrowed to 7V—14V by 1/2 IC2 (pins 1—3) on the voicing board to increase S/N ratio.

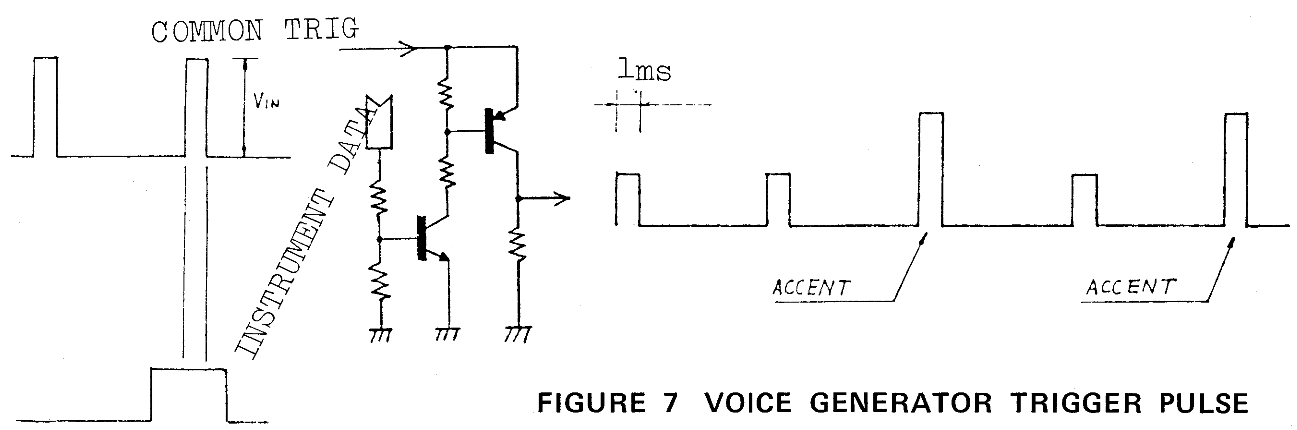


FIGURE 7 VOICE GENERATOR TRIGGER PULSE

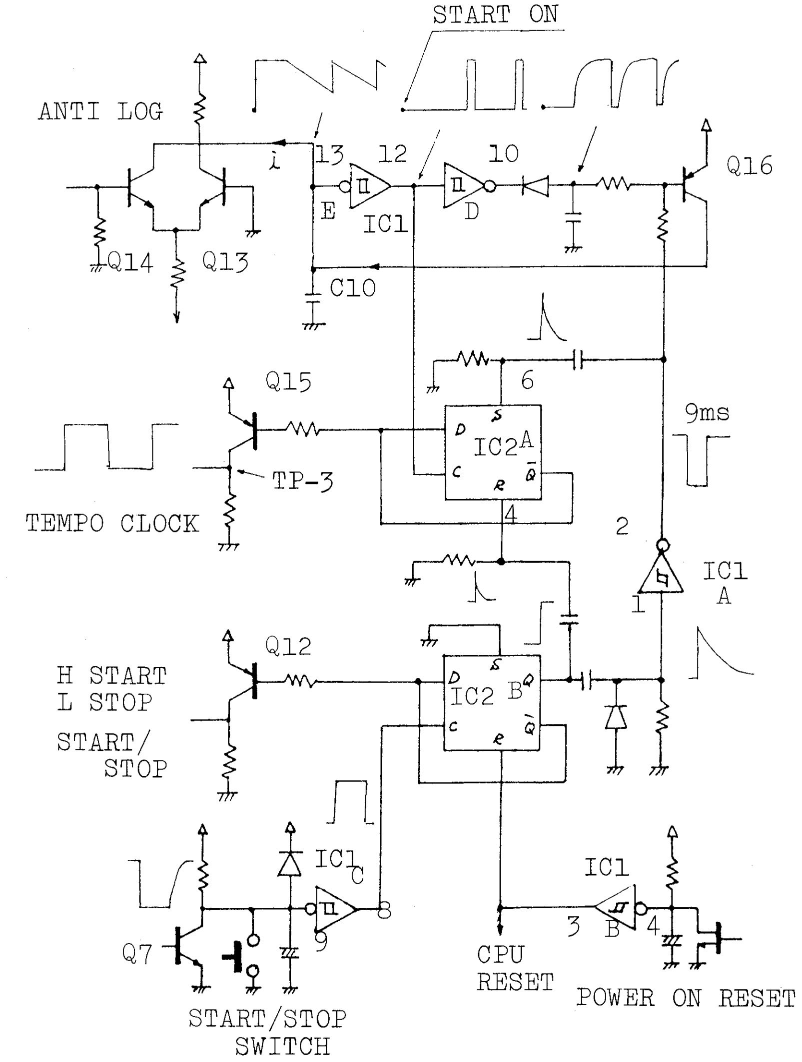


FIGURE 8 START/STOP & TEMPO CLOCK CIRCUITS

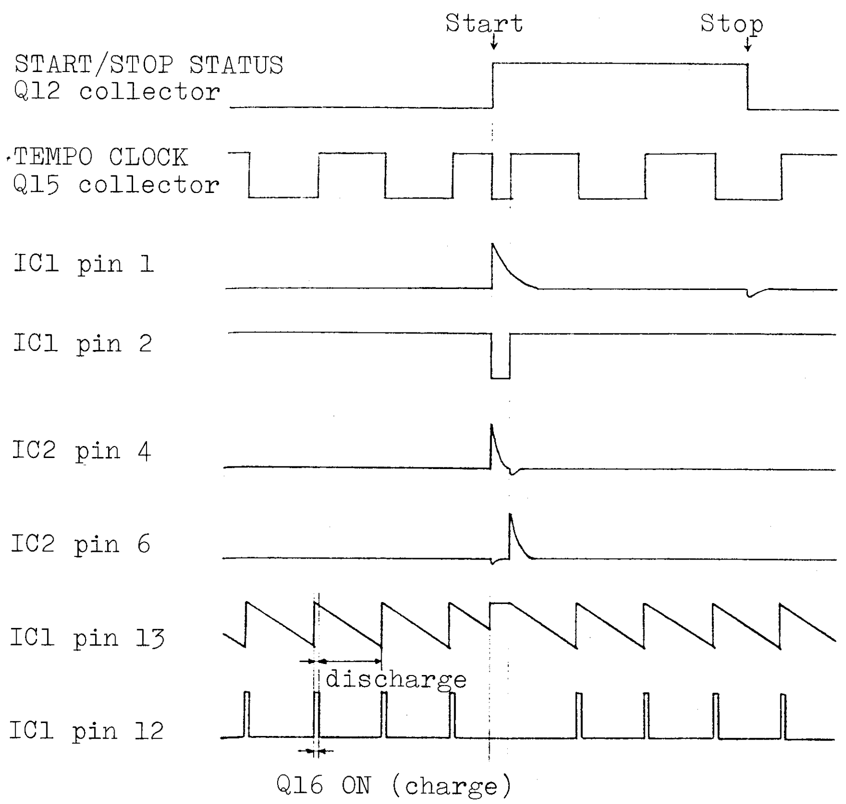


FIGURE 9 TEMPO CLOCK TIMING DIAGRAM

START/STOP & Tempo Clock

When the power supply for TR-808 is turned on, the TEMPO clock continues oscillation regardless of the operation mode of TR-808. However, when the START button is pressed in the STOP mode, oscillation stops once for 9ms to provide a mode change preparation time to CPU. In this way, the START/STOP circuit and the TEMPO circuit are closely related with each other. When the SYNC IN/OUT switch is set to IN, both circuits become ineffective and external signals from the DIN socket duplicate the both circuits.

When the START/STOP switch is pressed (closed) with rhythm stopped, $\bar{Q}$ of F/F IC2B becomes L, the collector of Q12 becomes H, Q of IC2B becomes H and IC2A is reset. $\bar{Q}$ of IC2A becomes H and the collector of Q15 becomes L. Then, since Q of IC2B becomes H, pin 2 of IC1 becomes L to turn on Q16. As a result, the TEMPO GENERATOR of 2/4 IC1 (D, E) stops oscillation (details are described later). After 9ms later, pin 1 of IC1A drops below the threshold level and pin 2 is reversed. The rising edge reverses $\bar{Q}$ of IC2A to L and the collector of Q15 (TEMPO CLOCK output) becomes H. At the same time, Q16 is cut off, and C10 starts discharging through the ANTI-LOG Q14 to continue oscillation.
This discharging speed of C10 determines the oscillation frequency of the TEMPO clock. The variation range is between 8.3ms and 65ms. With TR-808, ♩ is defined to have 24 clocks, and thus ♩ is approximately equal to 400—300.
When the level of C10 exceeds the threshold level of pin 13 of IC1 due to discharging, the output of pin 10 is reversed, Q16 turns on, and C10 is charged. The output of pin 12 of IC1 is divided into 1/2 by T-FF of IC2A.

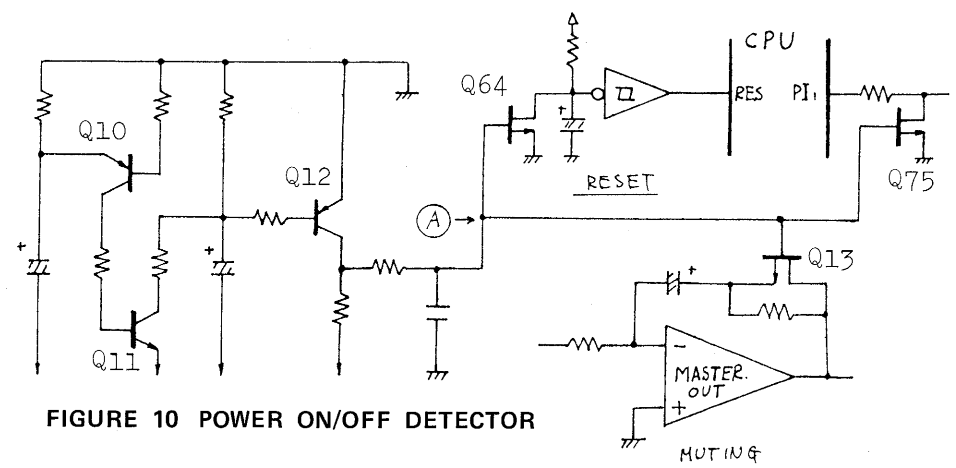


FIGURE 10 POWER ON/OFF DETECTOR

Muting, Reset

The circuit composed of Q10—Q12 detects power on/off or sharp voltage drops in TR-808 DC lines and feeds forward bias (0 volts) to FET switches connected to point A. These FETs are for resetting CPU (Q64), preventing writing into RAMs (Q75) and muting Master Out (Q13).

Power on: 0V 1-2sec —15V
Power off: —15V to 0V

If this circuit is defective, the CPU may be kept reset. (Detail in TROUBLESHOOTING on page 14.)

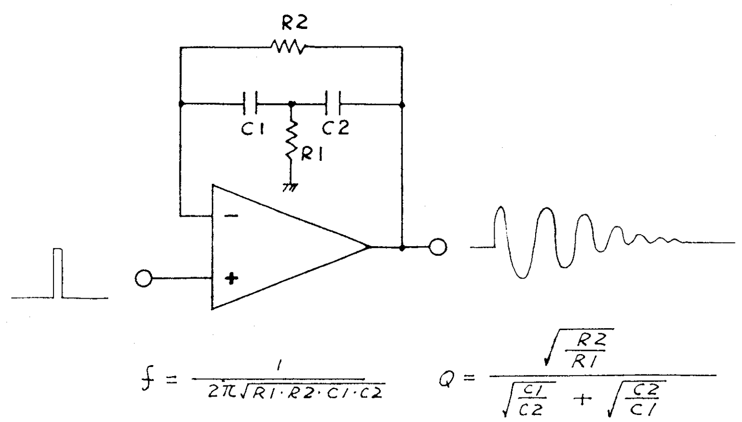


FIGURE 11 REPRESENTATIVE BRIDGED T-NETWORK

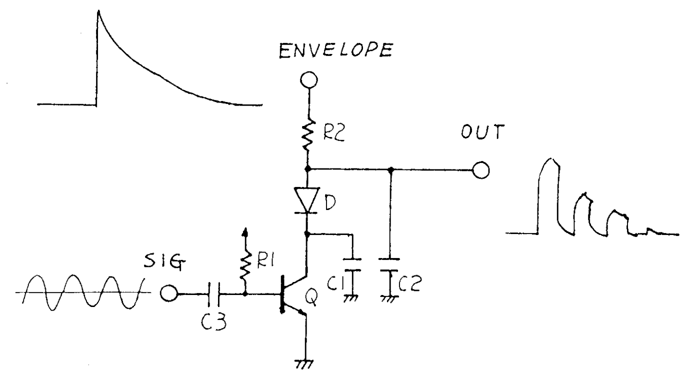


FIGURE 12 REPRESENTATIVE SWING TYPE VCA

Sound Generators

The bridged T-network filter shown in Fig. 11 is used to generate periodic damping drum sound. This configuration has variations according to application (instrument sound). Values of R and C can be changed. With this circuit, the decay time becomes longer as Q increases.

The swing type VCA shown in Fig. 12 is used to generate metalic sound (noise). This circuit features its output waveform having many high harmonic components to provide ringing metalic sound.

Major features of each sound generator are described below.

Bass Drum

This sound generator is composed of a multi-feedback, bridged T-network including 1/2 IC12 (pins 1—3) as an active element. The decay time of the resonating waveforms can be controlled by adjusting feedback amount by VR6.

Immediately after a trigger pulse is fed into the generator, the filter's time constant — when ACCENT is present — is halved and has a resonance on twice its inherent frequency for a half cycle period, then on the fixed frequency with decaying amplitude. This changing frequencies will sound a punchier crisp bass. This trick is performed by the circuit composed of Q41—Q43.

When a trigger signal is outputted from the collector of Q40, Q41 turns on, Q42 turns off, Q43 turns on and R165 is shorted. This halves the time constant of this network. The ON period of Q43 is determined by R156 and C38 and equals 4ms which is 1/2 x 1/2 of 16ms of the inherent oscillation period of the filter.
When Q42 turns on after 4ms, current discharging from C39 via R161 produces a retriggering pulse. At this time the generator oscillates on the inherent frequency.

Snare Drum

This sound generator has two bridged T-networks for fundamental waveforms and harmonic waveforms. The output ratio of the two can be changed by VR8 to tailor sound characteristic. The amplitude of snappy envelope can be controlled by VR9.

LT/LC (MT/MC, HT/HC)

These three sound generators are composed of the circuits based on the same principle. LT/LC is described below as an example.

This sound generator is composed of a multi-feedback, bridged T-network including IC5 as an active element. Voices are switched by SW8 (C77 – frequency, R224 – level). While the oscillation is large in amplitude immediately after triggering, it is on a higher frequency due to conductions of D80 and D81, which reduce time constant of the filter. As the resonance is damped, its frequency is lowered by the effect of increasing diodes' internal resistance. Timbre variations corresponding to time elapse will appreciably be heard as in the case of Bass Drum.

Pink noise with a slightly longer decay time is mixed for Low Tom Tom to provide artificial reveberation.

RS/CL

CL Output from multifeedback bridged T-network incorporated with IC20 is routed to IC19. Output from IC21 (for RS), also routed via R320, can be ignored because of its minimized level due to impedance imbalance at pin 7 of IC20b.

RS Disconnected R313 makes IC20b just as a buffer for CI20a output. The output of IC20b is applied to Q62 together with the output of IC21. The envelope applied to Q62 is formed by R107 and C24. As described in the beginning of this section, VCA of this type is intended to provide many high harmonics in the output signals.
Normally-conducting Q74 remains off only while trigger pulse is transferred from Q61 to allow IC19 to pass signals. This switching is provided to eliminate noise leaking from IC20, especially for CL – relatively large amount, being wired for high Q.

CP/MA

White noise passed through the band pass filter (IC21) is applied to two VCAs in parallel to have different envelopes. These envelopes are combined to obtain sound source for the CP sound generator.
Since an envelope with a relatively long decay time is applied to the VCA Q70, output from this VCA constitutes reverberation of CP sound.
The output envelope at the VCA (IC22, Q71 and Q72) is a unique sawtooth shape, and is a main component of this sound generator.
The sawtooth envelope generator circuit is mainly described below to explain its rather complicated operation. When trigger pulses are applied to pin 8 of the quad comparator IC23, the output is integrated by R350 and C140, and converted into pulses of 30ms wide as shown in Fig. 13-2. At the falling edge of the pulse, pin 13 of IC23 becomes H (Fig. 13-3). The output from pin 1 of IC23 is also applied to pin 4 of IC23, pin 2 of IC23 becomes from –15V to 0V,

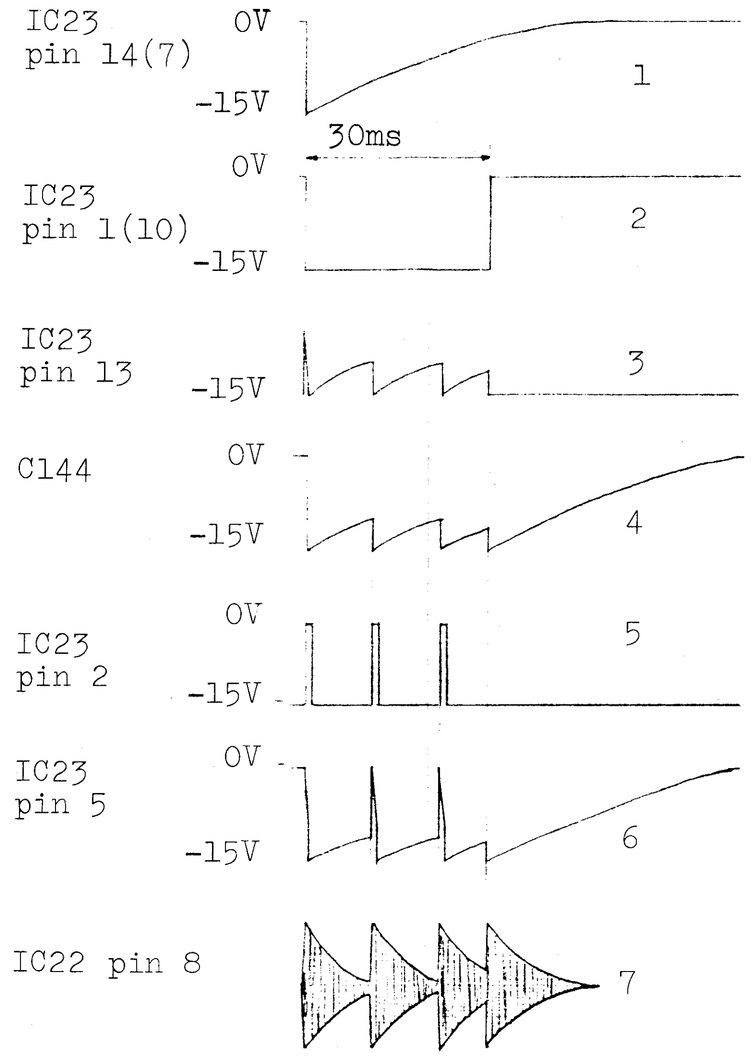


FIGURE 13 HAND CLAP GENERATING CYCLE

Q73 turns on, pin 5 of IC23 becomes –15V, pin 2 of IC23 returns to –15V, and Q73 returns to off state. Accordingly, the output waveform at pin 2 of IC23 becomes narrow pulses as shown in Fig. 13-5.
The moment Q73 is turned on, C144 is abruptly charged to –15V. However, immediately after charging, Q73 turns off and the charges are discharged through R365 and D71. When the level of pin 5 of IC23 becomes higher than the level of pin 4 due to discharging, pin 2 of IC23 reverses again and C144 is recharged to –15V. After this process is repeated and advanced to the middle of the third time, pin 1 of IC23 rises to 0V. This signal is differenciated by R357 and C141, and the generated pulse turns on Q73. At this time, although the terminal voltage of C144 rises gradually from –15V due to discharging, pin 2 does not reverse since pin 4 of IC23 has reached 0V. The output (Fig. 13-4) of this envelope generator is applied to the base of Q72 and converted exponentially by Q72 together with the signals applied to the base of Q71 (offset adj. signal from TM3 and accent signal via D68, C143 and R362. The converted signal is applied from the collector of Q72 to pin 1 of IC22 to change the amplitude of noise from the filter IC21.

Note: IC23 (AN6912) is constructed with open collector NPN transistors for output and operates on single (negative) power only.

MA White noise is gated by Q65 and supplied to the same buffer IC19 as for the CP sound generator through the filter Q68. Envelope for MA sound generator is generated by Q66 and Q67.

CB

This sound generator uses the outputs of two square waveform oscillators with different frequencies (by Schmitt triggers). Each oscillation output passes the corresponding exclusive gate (VCA, Q14, Q15) and mixed by the filter IC2.

A series of R82 and C34 connected in parallel with C9 forms an envelope having abrupt level decay at the initial trailing edge to emphasize attack effect.

CY

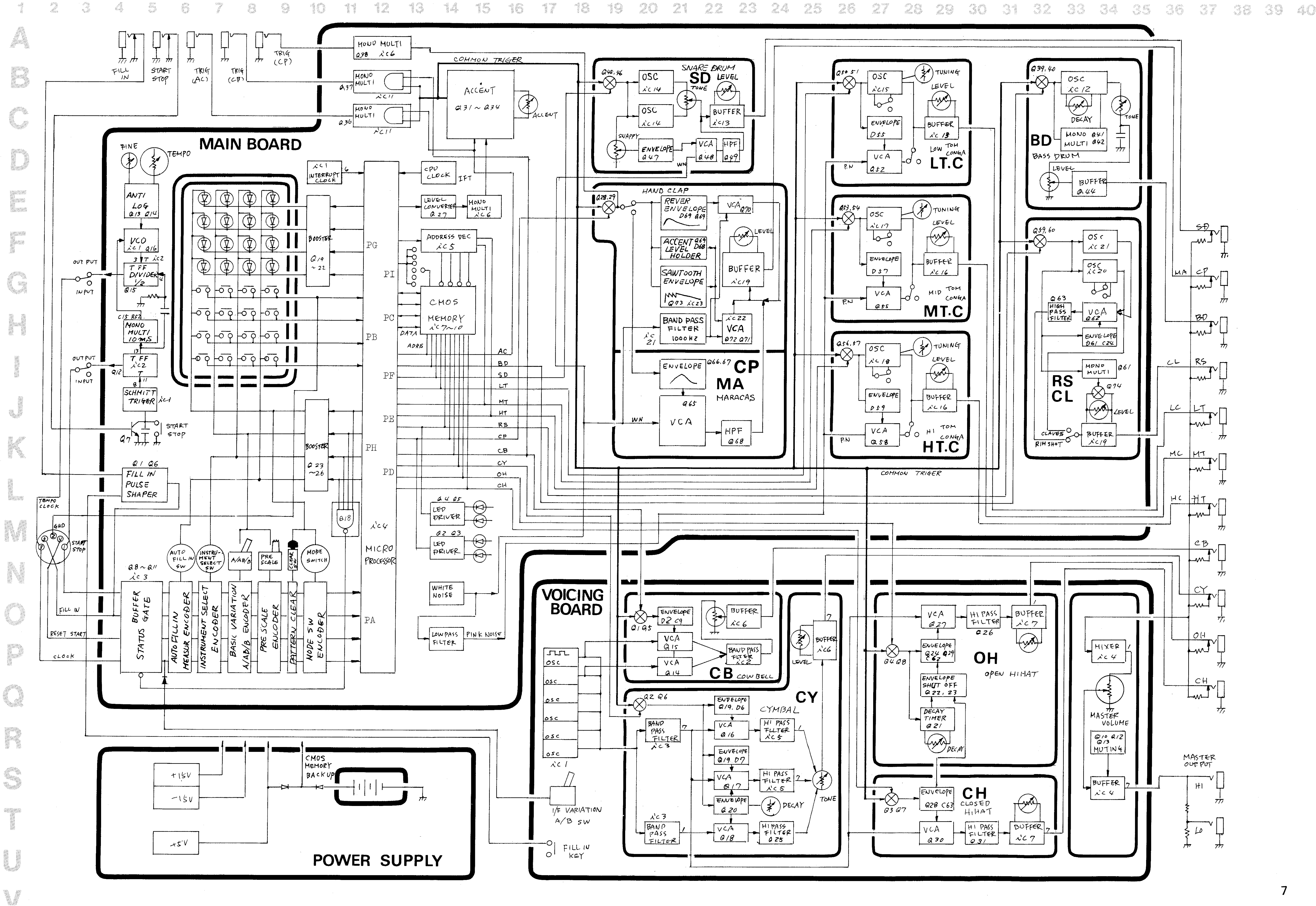
The combined square wave outputs of six Schumitt triggers including two for CB generator is separated into high and low range components by two filters composed of IC3. The high range component from pin 7 of IC3 is further separated into two frequency ranges. The output of the gate Q16 has the highest frequency component of this sound generator. Its decay time is short. The output of Q17 is in a frequency range slightly lower than the above output, and its decay time is controllable.
These three signals with different frequency ranges are outputted with their level ratio controlled by VR4.

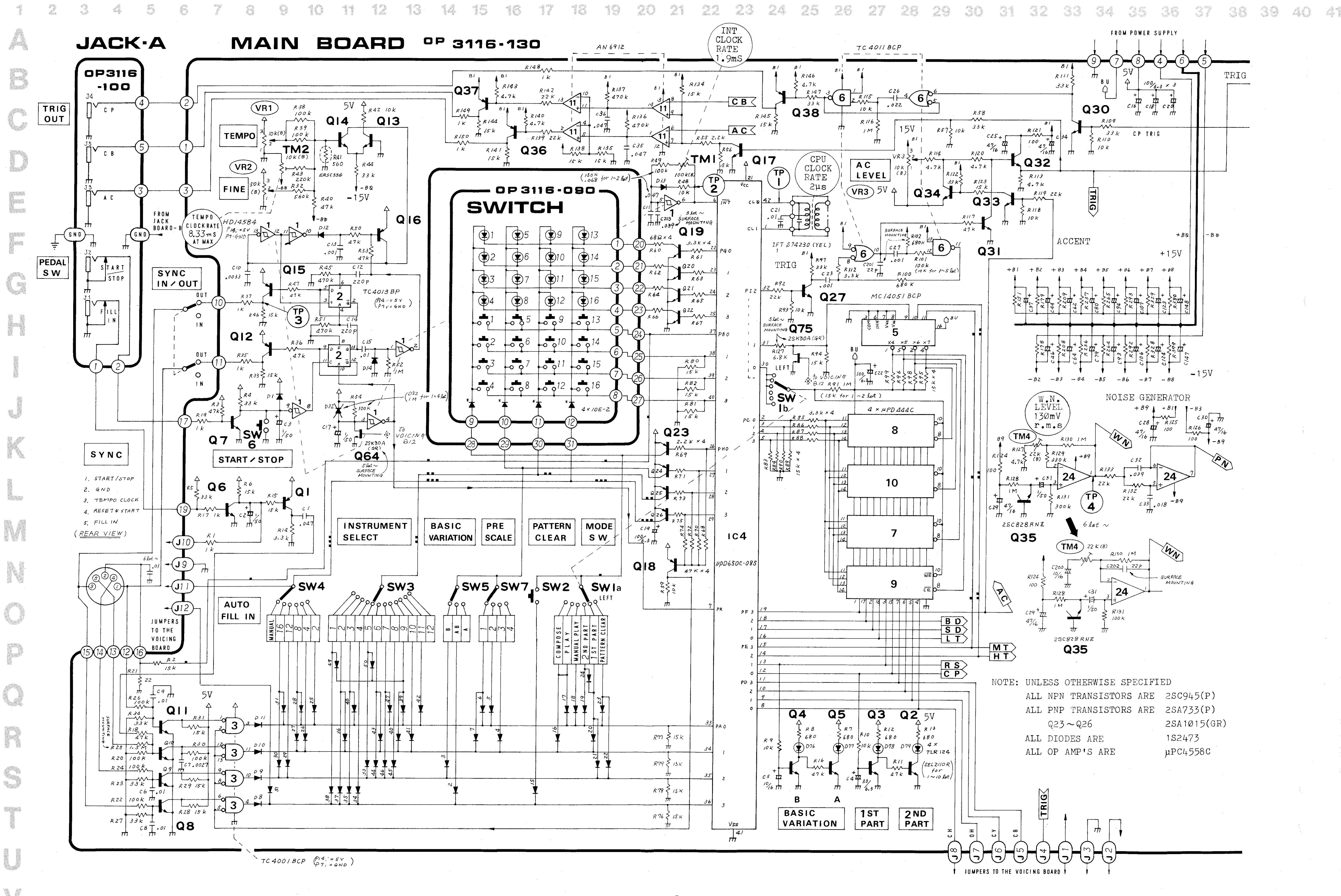
OH

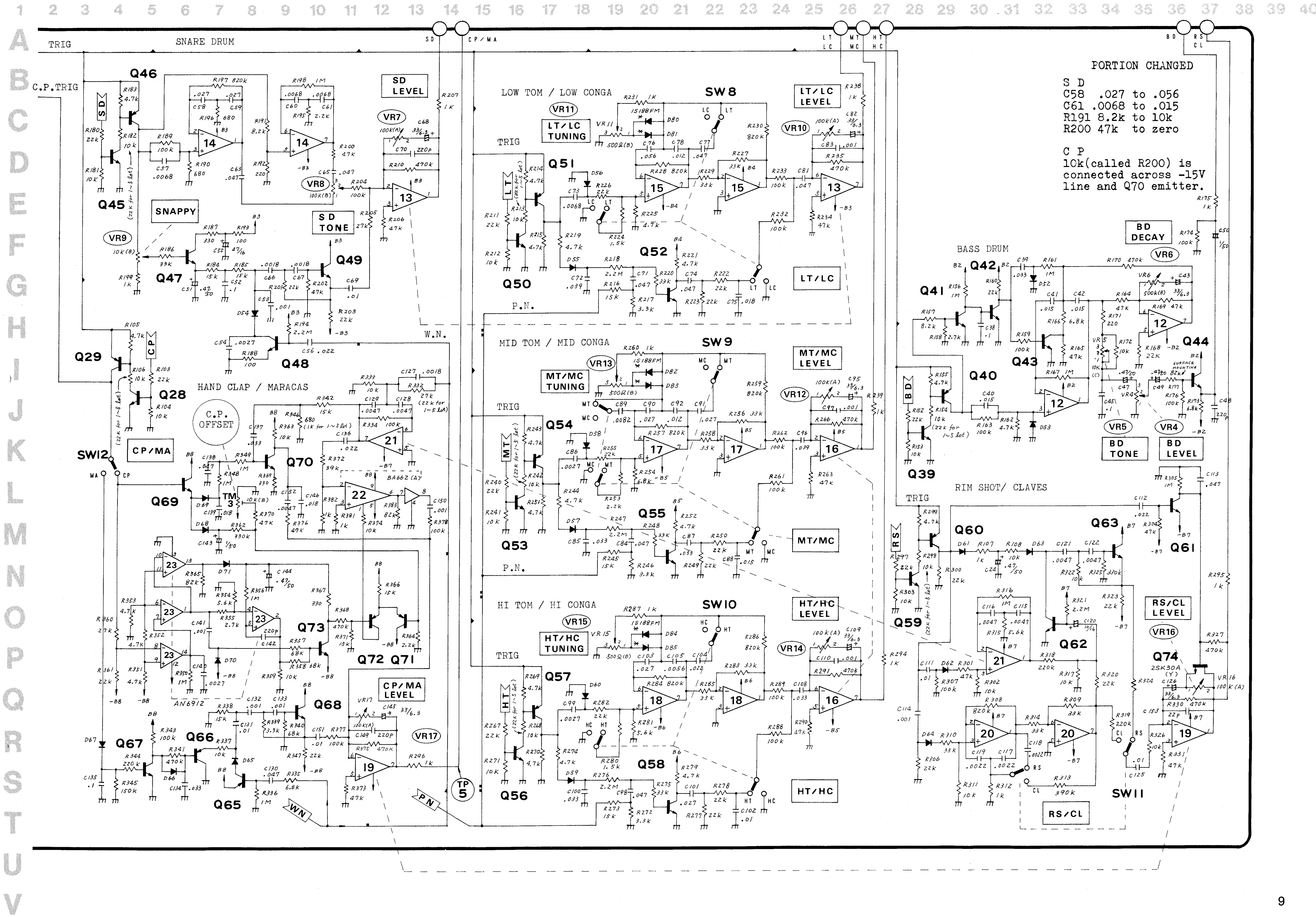
The high frequency range component signal obtained by the above 1/2 IC3 is gated by Q27 and supplied to the buffer IC7 through the filter Q26. When the CLOSED HI-HAT (CH) is triggered while the OH circuit is activated, Q23 turns on by the voltage applied through R173. At this moment, the decay time of the OH circuit terminates.

CH

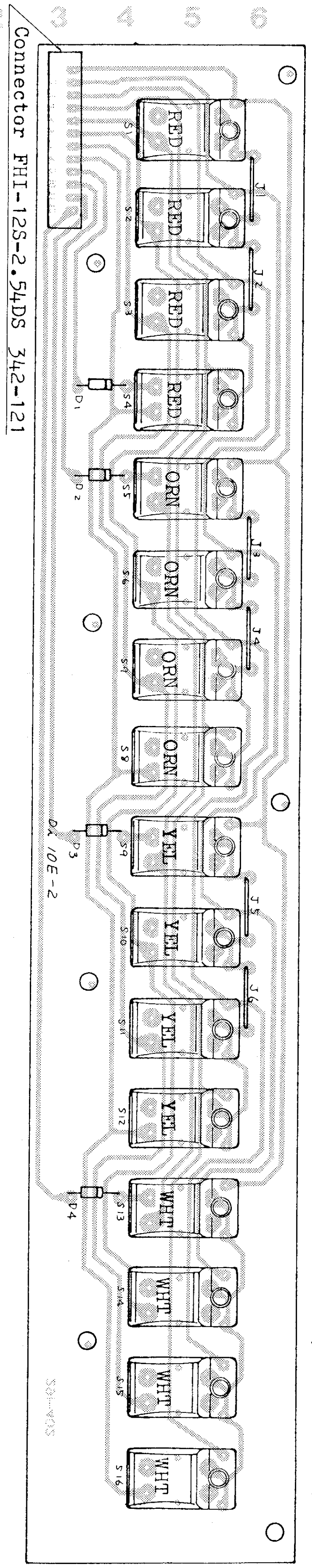
This shares the same sound source with the OH. The signal is gated by Q30 and supplied to the filter Q31 and the buffer IC7 (1/2).


MAIN BOARD
VOICING BOARD
POWER SUPPLY
SD
SNARE DRUM
CP
HAND CLAP
MA
MARACAS
LT.C
MT.C
HT.C
BD
BASS DRUM
RS
CL
CB
COW BELL
CY
CYMBAL
OH
OPEN HIHAT
CH
CLOSED HIHAT
ACCENT
COMMON TRIGER
CMOS MEMORY
MICRO PROCESSOR
WHITE NOISE
PINK NOISE
MASTER VOLUME
MASTER OUTPUT
+15V
−15V
+5V
CMOS MEMORY BACK UP
FILL IN KEY
I/F VARIATION A/B SW
START STOP
TEMPO
FINE


JACK·A
MAIN BOARD OP 3116-130
OP3116 -100
TRIG OUT
PEDAL SW
SYNC IN / OUT
SYNC
1. START/STOP
2. GND
3. TEMPO CLOCK
4. RESET & START
5. FILL IN
(REAR VIEW)
TEMPO
FINE
VR1
VR2
TM2
TEMPO CLOCKRATE 8.33mS AT MAX
INT CLOCK RATE 1.9mS
CPU CLOCK RATE 2μs
OP 3116-090
SWITCH
START / STOP
INSTRUMENT SELECT
BASIC VARIATION
PRE SCALE
PATTERN CLEAR
MODE SW
AUTO FILL IN
JUMPERS TO THE VOICING BOARD
SW4
SW3
SW5
SW7
SW2
SW1a
SW1b
AC LEVEL
VR3
TM1
TRIG
ACCENT
FROM POWER SUPPLY
NOISE GENERATOR
W.N. LEVEL 130mV r.m.s
TM4
IC4
μPD650C-085
4 × μPD444C
MC14051BCP
TC4013BP
TC4011BCP
TC4001BCP
HD14584
AN6912
BASIC VARIATION
1ST PART
2ND PART
COMPOSE
PLAY
MANUAL PLAY
2ND PART
1ST PART
PATTERN CLEAR
MANUAL
JUMPERS TO THE VOICING BOARD
NOTE: UNLESS OTHERWISE SPECIFIED
ALL NPN TRANSISTORS ARE 2SC945(P)
ALL PNP TRANSISTORS ARE 2SA733(P)
Q23~Q26 2SA1015(GR)
ALL DIODES ARE 1S2473
ALL OP AMP'S ARE μPC4558C


TRIG
SNARE DRUM
C.P.TRIG
SD LEVEL
SNAPPY
SD TONE
HAND CLAP / MARACAS
C.P. OFFSET
CP/MA
CP/MA LEVEL
LOW TOM / LOW CONGA
LT/LC TUNING
LT/LC LEVEL
LT/LC
MID TOM / MID CONGA
MT/MC TUNING
MT/MC LEVEL
MT/MC
HI TOM / HI CONGA
HT/HC TUNING
HT/HC LEVEL
HT/HC
P.N.
W.N.
BASS DRUM
BD DECAY
BD TONE
BD LEVEL
RIM SHOT/ CLAVES
RS/CL LEVEL
RS/CL
PORTION CHANGED
S D
C58 .027 to .056
C61 .0068 to .015
R191 8.2k to 10k
R200 47k to zero
C P
10k(called R200) is
connected across -15V
line and Q70 emitter.

SWITCH BOARD
OP3116·090 (7311609000)
(pcb 291-402)

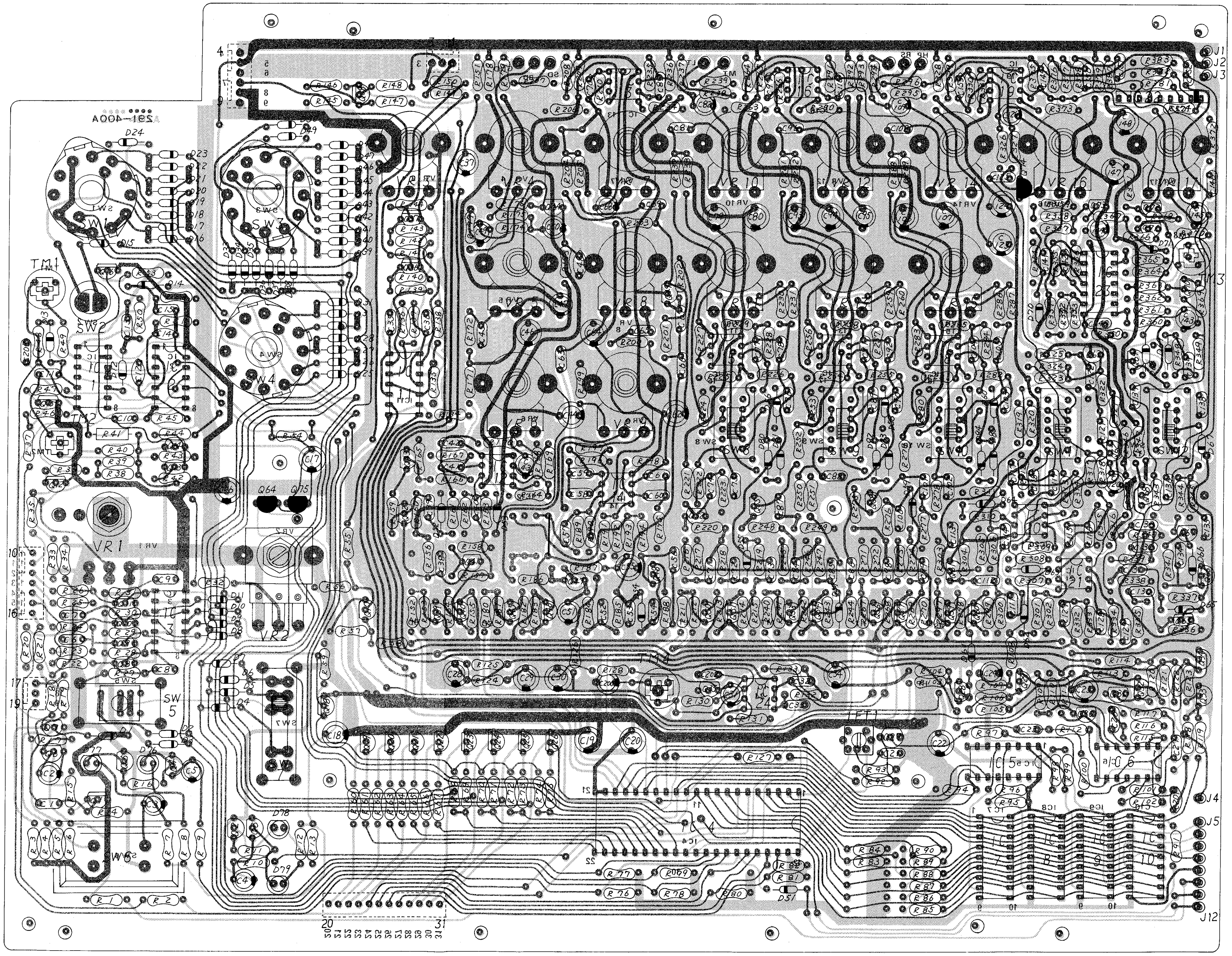


SWITCH

SW KHC11901(RED) 316-601, Key Top 247-167(WHT),247-168(ORN),247-169(YEL),247-180(RED)

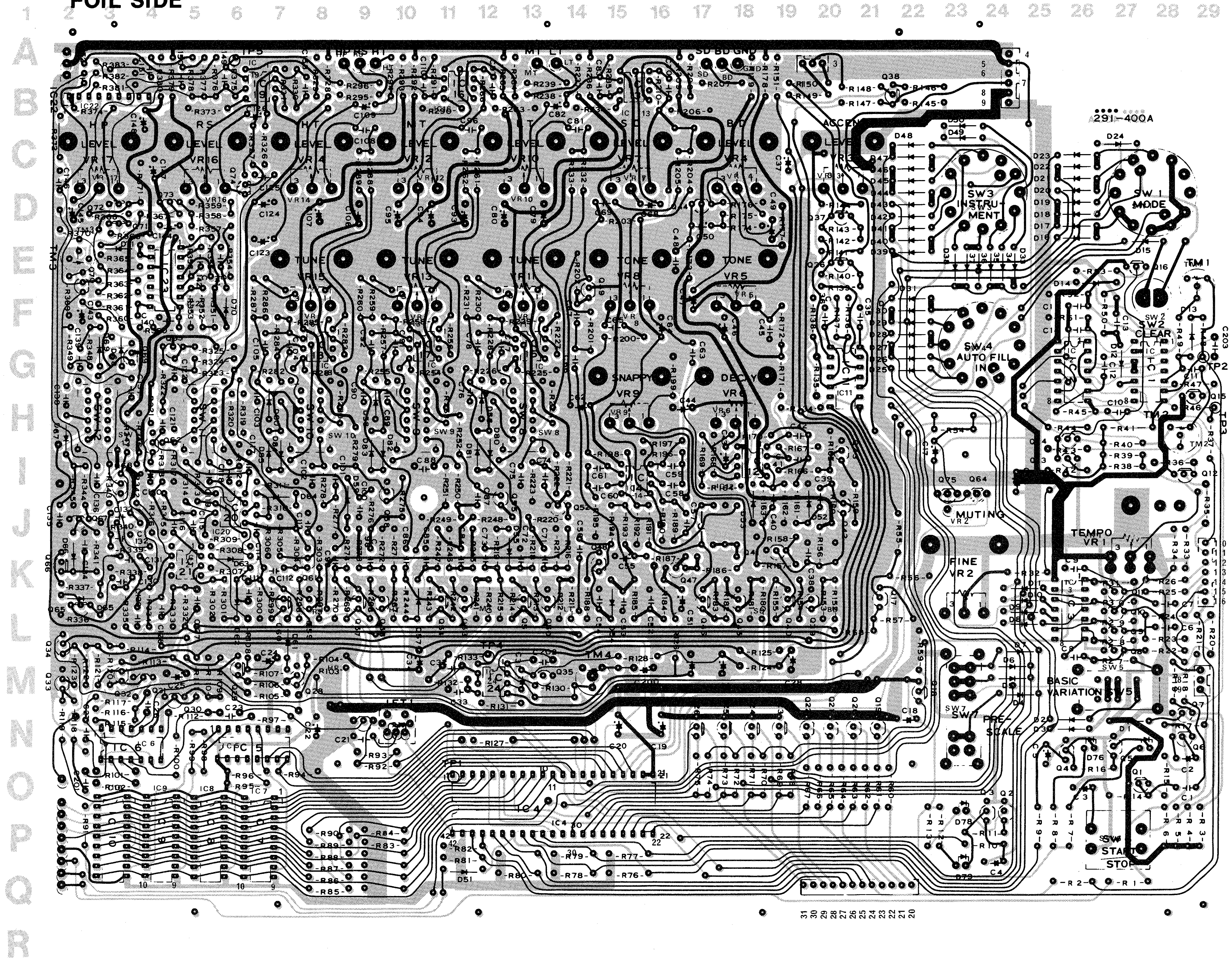
MAIN BOARD
OP3116-130 (7311613006)
(pcb 291-400A)

COMPONENT SIDE

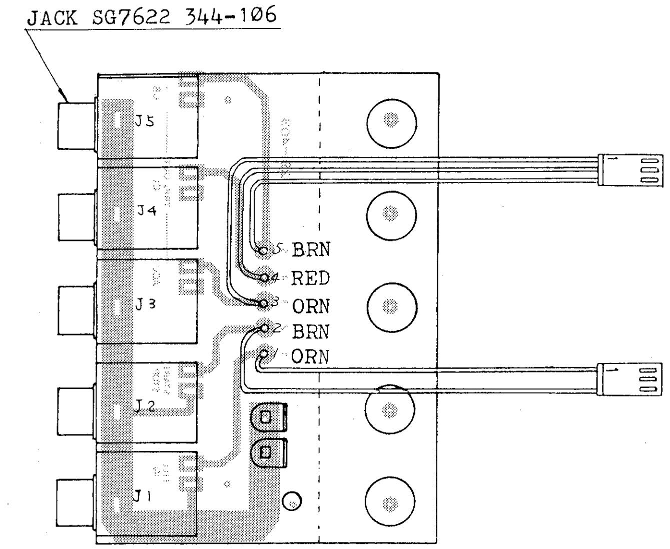


MAIN BOARD
OP3116-130 (7311613006)
(pcb 291-400A)

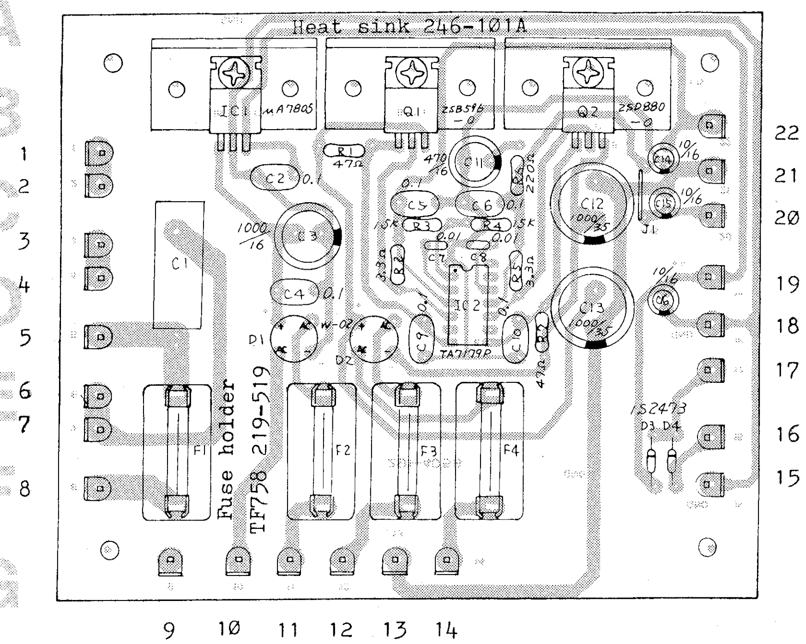
FOIL SIDE



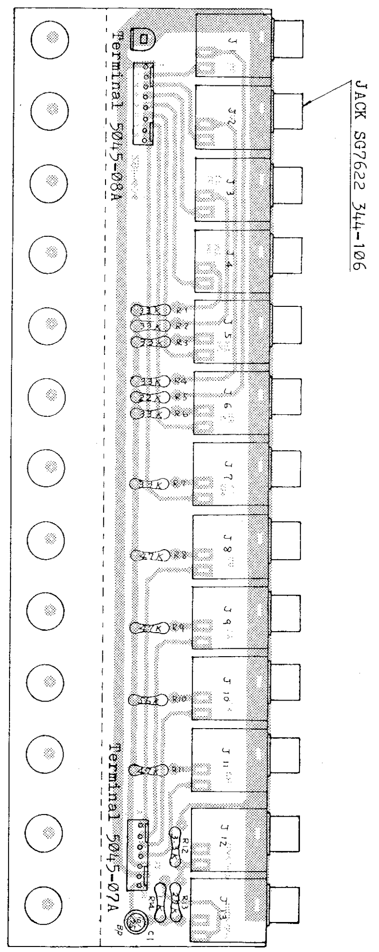
JACK BOARD A
OP3116-100 (7311610000)
(pcb 291-403)



POWER SUPPLY
PS3116-051 (7311605100) 100/117V
PS3116-054 (7311605400) 220/240V
(pcb 291-405A)

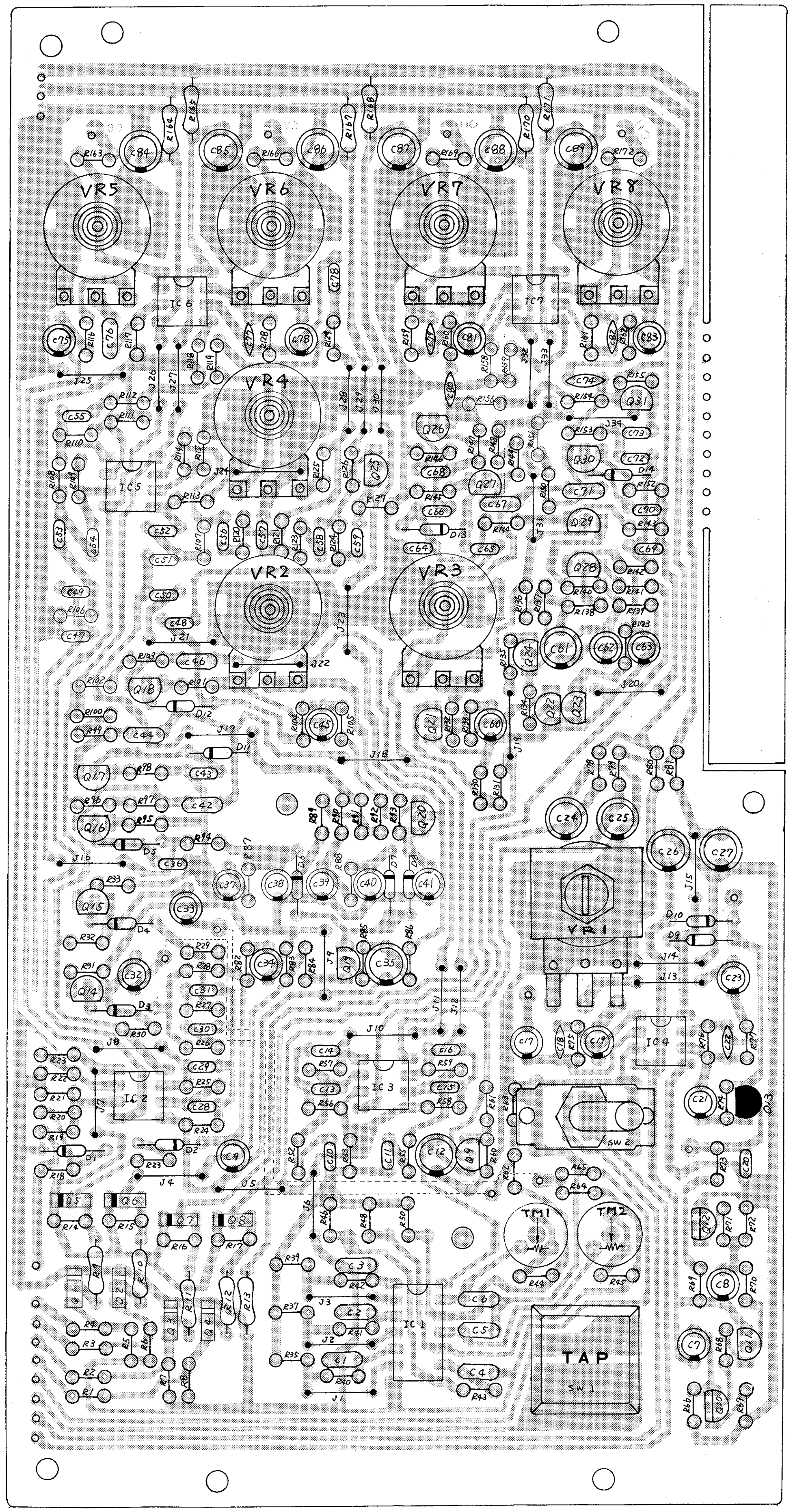


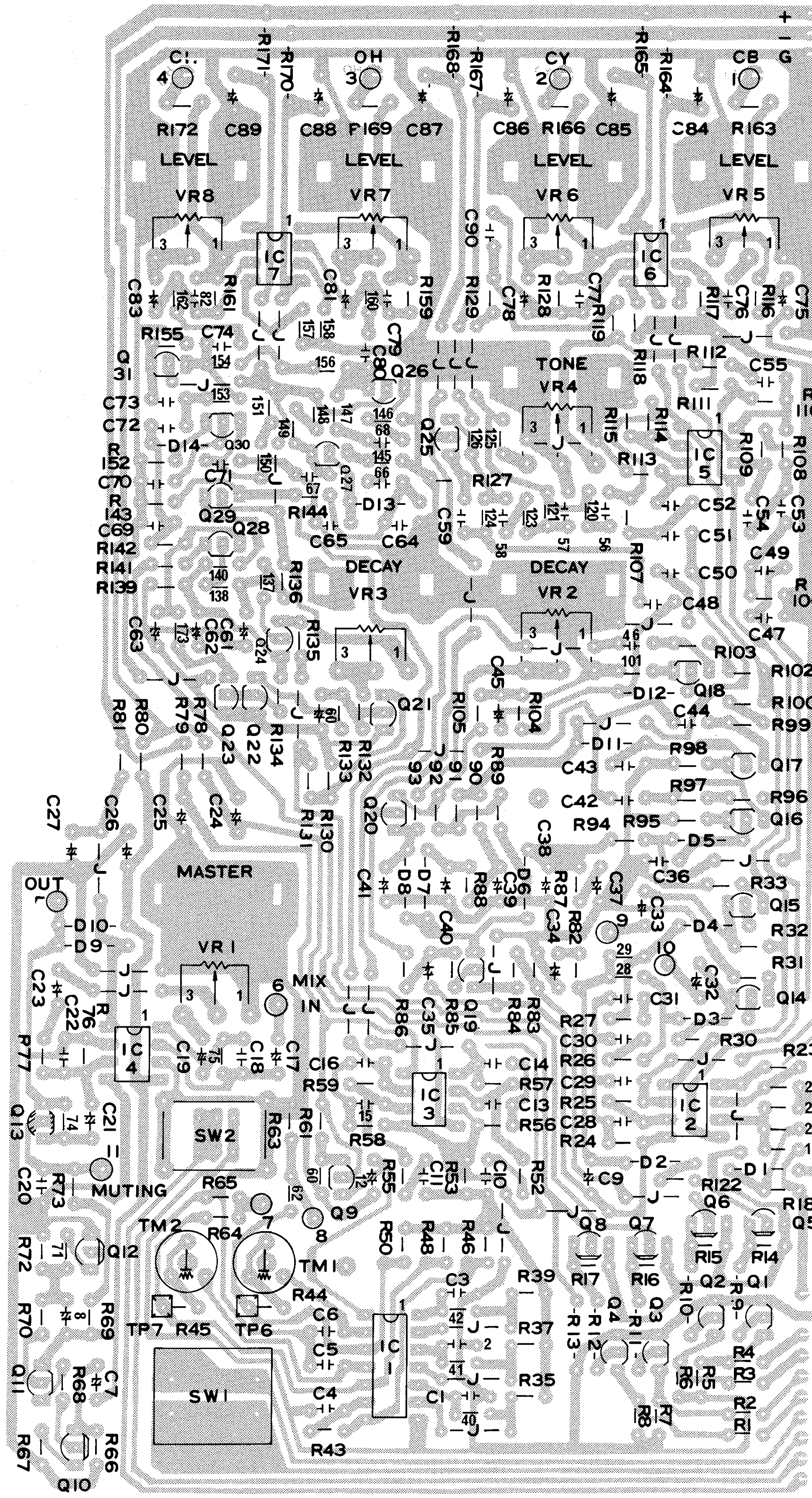
JACK BOARD B
OP3116-110 (7311611000)
(pcb 291-404)

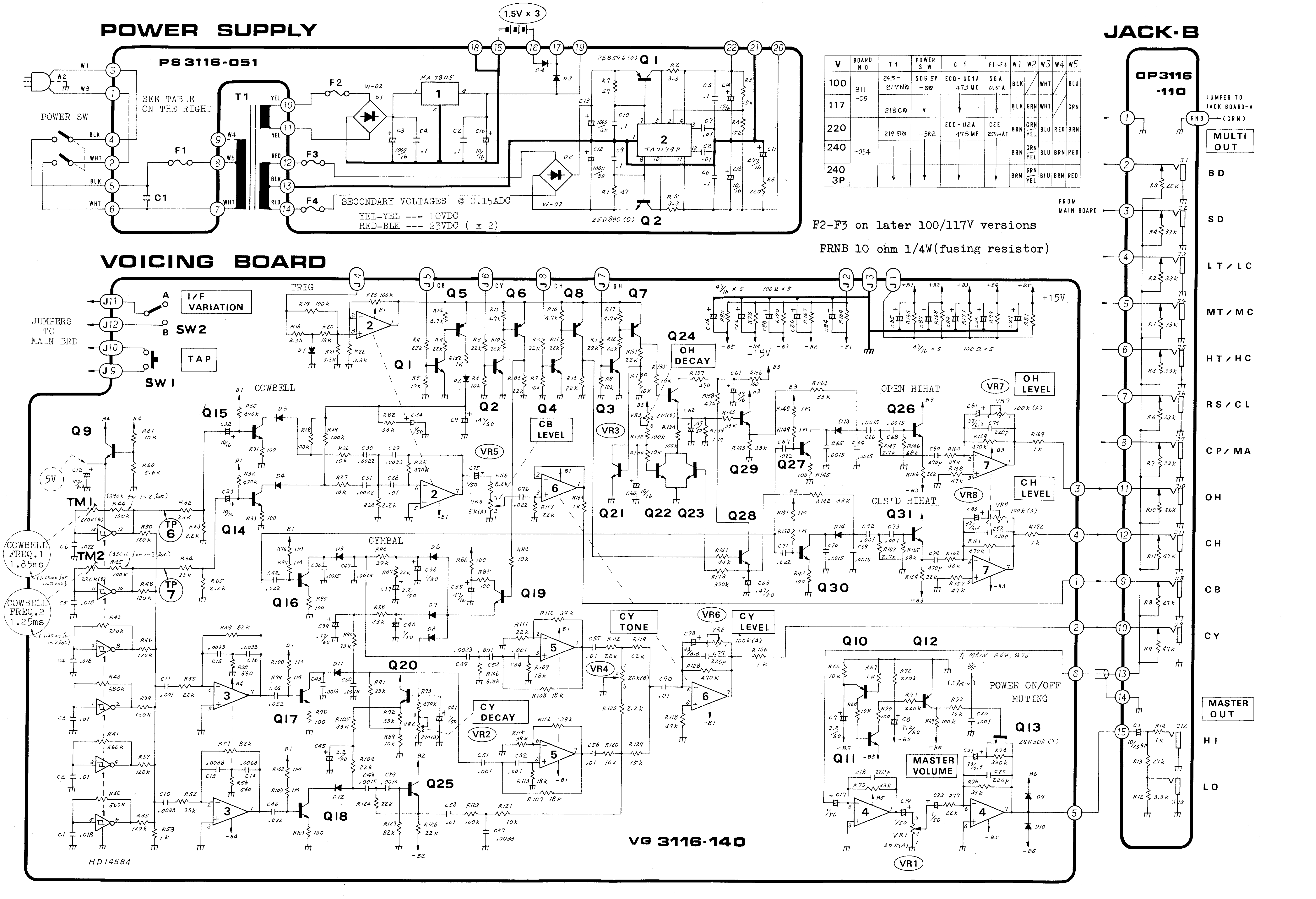


COMPONENT SIDE **VOICING BOARD VG3116-140 (7311614001)** FOIL SIDE

(pcb 291-401A)





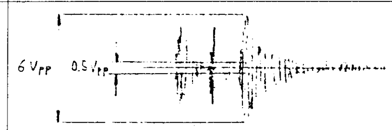


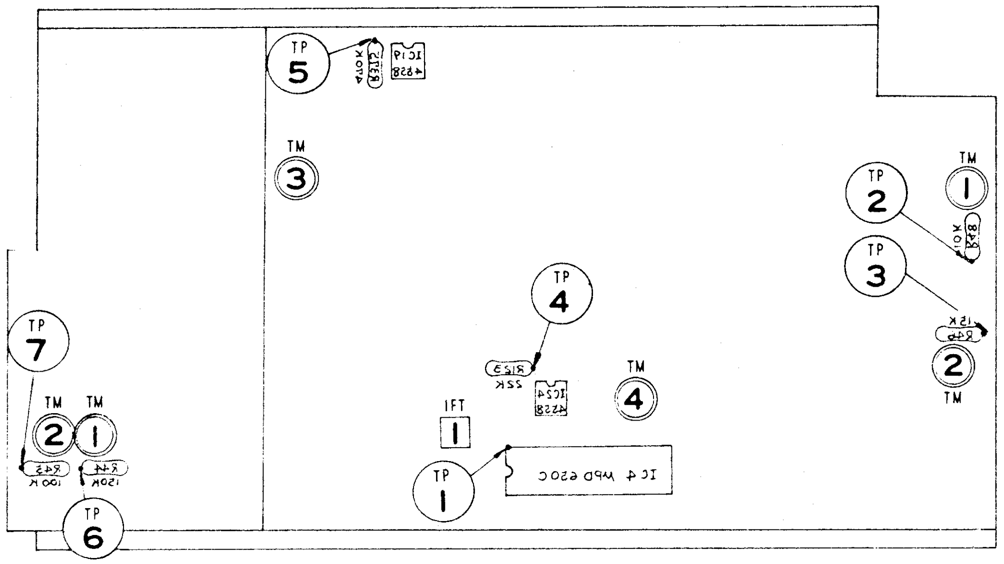
V	BOARD NO	T1	POWER SW	C1	F1~F4	W1	W2	W3	W4	W5
100	311-051	245-217NO	SDG 5P -001	ECO-UC1A 473MC	SGA 0.5A	BLK	/	WHT	/	BLU
117		218CO	↓	↓	↓	BLK	GRN	WHT	/	GRN
220	-054	219DO	-502	ECO-U2A 473MF	CEE 250mAT	BRN	GRN/YEL	BLU	RED	BRN
240		↓	↓	↓	↓	BRN	GRN/YEL	BLU	BRN	RED
240 3P		↓	↓	↓	↓	BRN	GRN/YEL	BLU	BRN	RED

F2-F3 on later 100/117V versions

FRNB 10 ohm 1/4W(fusing resistor)

ADJUSTMENT

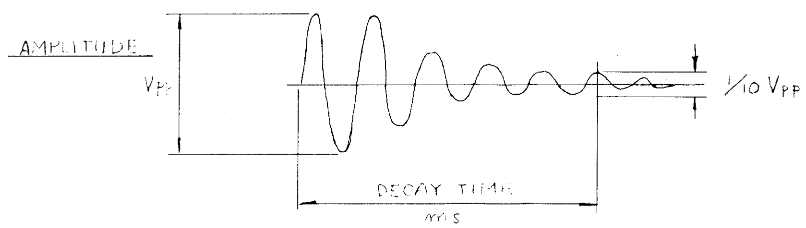
ADJUSTMENT	Connect	Set	Adjust	Reading
CPU CLOCK	scope to TP-1		IFT-1	2us/cycle(500kHz)
			check	4V p-p
INT CLOCK	scope to TP-2		TM-1	1.9ms/cycle
TEMPO CLOCK	scope to TP-3	TEMPO.FINE:FCW	TM-2	8.33ms/cycle
		TEMPO: FCCW FINE: FCW	check	65ms±5ms/cycle
NOISE GENERATOR	AC volt-meter to TP-4		TM-4	130mV rms
CP (HAND CLAP) OFFSET	scope to TP-5	write, play CP at a tempo w/ LEVEL FCW	TM-3	
CB (COW BELL) FREQUENCY	scope to TP-6		TM-1	1.85ms/cycle
	TP-7		TM-2	1.25ms/cycle



CHECKING VOICES

- Refer to right-hand table -

Connect scope to the MULTI OUT jack of a VOICE.
When observing amplitude, set ACCENT LEVEL to FCCW position and the VOICE LEVEL to FCW, then turn ACCENT FCW. DECAY, TONE, etc. for that voice must be set at 12 o'clock.



		AMPLITUDE		FREQUENCY			DECAY TIME		
		NORMAL	ACCENT	LOW	MID	HIGH	SHORT	MID	LONG
		Vpp	Vpp	ms (Hz)	ms (Hz)	ms (Hz)	ms	ms	ms
BD		3.5	10	—	18 (56)	—	50	300	800
SD	H	3	10	—	2.1 (476)	—	—	60	—
	L				4.2 (238)				
LC		3.5	12	6.1 (165)	5.4 (185)	4.5 (220)	—	180	—
LT		3.5	12	12.5 (80)	11.1 (90)	10 (100)	—	200	—
MC		3	10	4 (250)	3.6 (280)	3.2 (310)	—	100	—
MT		3	11	8.3 (120)	7.4 (135)	6.3 (160)	—	130	—
HC		3.5	12	2.7 (370)	2.5 (400)	2.2 (455)	—	80	—
HT		3.5	12	6.1 (165)	5.4 (185)	4.5 (220)	—	100	—
C		2.5	8	—	0.4 (2500)	—	—	25	—
RS	H	3	10	—	0.6 (1667)	—	—	10	—
	L				2.2 (455)				
M		3	5	—	—	—	25	—	35
CP		6	2	—	—	—	—	100	—
CB	H	3.5	12	—	1.25 (800)	—	—	50	—
	L				1.85 (540)				
CY		3.5	7	—	—	—	350	800	1200
OH		3.5	7	—	—	—	90	450	600
CH		3	6	—	—	—	—	50	—

values are typical and variable

TROUBLESHOOTING

This section describes fundamental approach to isolate defective circuits or components.
Although most TR-808 circuits function under the CPU control, possible reasons will often be found on peripheral circuits. Replace CPU last of all.
Some useful information can be derived from the circuit description.

DC SUPPLY

Confirmation of DC supply voltages is the first thing to be done in troubleshooting. Check +5V, ±15V and back-up. CPU is forced to reset and is not allowed to restart when DC source is so irregular that Voltage Change Detector keeps reset signal.
Lower impedance load connecting to voice output jack can draw relatively large current through op amp when the sound level is high. The sum of the currents, when many louder voices are outputted in step, flowing into these loads would cause DC source to drop enough below the Detector sensing level. To make sure of this, pull all plugs off the jacks. Contrast to the above is a short-circuitting IC. One short circuit in a stage only could not be sensed by the detector since "B" supplied to a particular circuit group is independently filtered, or rather, the short circuit will increase ripples in the line, causing TEMPO CLOCK to be unstable.

STATUS, SWITCH SCANNING

Each port at PH routes scanning signal to the switches connecting to its bus. PA and PB read signals coming via the switches. If a switch is misread, check scannings for other switches: one sharing the same PH bus, one sharing the same input port - with corresponding switchings.

RAM STORED DATA

As shown in memory map on page 4, a RAM is partitioned into blocks. It is unlikely to occur in a RAM that only one block fails to handle data when the RAM or the Decoder malfunctions. For example, if all instrument data but Cow Bell enter IC8, similar phenomenon might true to other RAMs, were the troubles through PC-0 bus.

TRIGGER PULSE

Lack of trigger pulse from a gate is not what Common Trig is responsible for, when other sound generators are fired.
Common Trig with pulse width longer or shorter than 1ms will be a cause of deteriorative voices.

DESIGN CHANGES & IMPROVEMENTS

The reasons for modifications will help to remedy the problems as described below, may be found on early TR-808.
Some of the modifications were done at the factory on some products bearing serial number earlier than indicated:

MAIN BOARD - modification 1, 4
VOICING BOARD - modification 1

MAIN BOARD

	EFFECTIVE WITH SERIAL NUMBER	PART AFFECTED	REASON (* SOLUTION)
1	000300	INT CLOCK IC1 (HD14584) C11 0.068 → 0.047 / → 0.039 (C203)	Variations in HD14584 hysterisis sometimes deviate Clock Rate out of specified frequency range. * To down - 0.047+0.039 in parallel * To up - remove 0.039
2	010600	CP (Hand Clap) IC21 R346 1K → 680 R332 22K → 27K	CP sound overmatches the rest in level. * Reduce the gain (Both proper and reverberation components.)
3	010600	CPU (pin 30) R91 15K → 1M	Small resistance allows CPU to draw relatively larger current from back-up batteries with MODE selected other than PLAY or MANUAL PLAY in Power OFF. * Increase resistance
4	010600	DIN SOCKET (pin 5) R25 220K → 1.5M	Reject unnecessary signals from external circuitry to prevent false triggering at subsequent stage. * Increase resistance
		CPU (pin 37) Capacitor 0.01 across DIN pin 2 and chassis Grounding	Protect CPU against static electricity build-up at external circuitry. * By pass charge
5	010600	NOISE GENERATOR (IC24) R129 330K → short R311 330K → 100K R127 4.7K → 10u (C200) C202 0 → 22p	Variations in UPC4558 bias current are transferred to 1/2 IC24 output as an offset reducing gain margin. * Decouple DC

MAIN BOARD cont'd

	EFFECTIVE WITH SERIAL NUMBER	PART AFFECTED	REASON (* SOLUTION)
6	010600	VOICE GATE R106, R154, R182, R213, R242, R268, R298 22K → 10K	Ensure sufficiency of gate drive signal voltage at lower COMMON TRIG amplitude. * Increase gain
7	010600	COMMON TRIG IC6 (TC4011BP) R101 10K → 100K C201 0 → 22p	High frequency from CP generator induces irregular oscillation on other generators triggered at the same time. * Filter out CP high frequencies
8	020800	START/STOP (IC2) CPU (pins 7, 31) Q64,Q75 0 → FET R127 0 → 6.8K R54 1M → 100K D32 1 → 0	Prevent possible disturbance in RAM memories at power on/off switchings with MODE set at other than PLAY or MANUAL PLAY. * Add FET switches
9	031100	LED SEL2110R → TLR124	Eliminate possible chance of LED D76(D78) being lit by base current of Q5(Q2). * Use low sensitive LED

VOICING BOARD

	EFFECTIVE WITH SERIAL NUMBER	PART AFFECTED	REASON (* SOLUTION)
1	000300	COW BELL (IC1) C6 0.01 → 0.022 R44 390K → 150K R45 330K → 100K	Difficulty in setting COW BELL sound frequency within the specified range. * Extend TM1 and TM2 control range
2	010500	Q1-Q4 2SC945P → 2SC2021R	To have a clearance between Switch Board and transistors' top. * Employ transistors in shorter package
	051850	Q5-Q8 2SA733P → 2SA937Q	

PARTS LIST

PANEL

2221024200	Panel	N-242	top	–
2112511800	Panel	N-118	side (L, H)	(066H021)
2112511900	Panel	N-119	side (R, H)	
2281023401	Chassis	N-234		–
111-021	Rubber Foot G-5		rear	–
111-023	Rubber Foot G-7		front	–

SOCKET

13429604	Din connector	TCS0250-01-03		–
13449106	Jack	SG7622	#8 mono	(009-012)

TRANSFORMER COIL

22450217NO	Power transformer	N-217N	100V	–
22450218CO	Power transformer	N-218C	117V	–
22450219DO	Power transformer	N-219D	220/240V	–
12449217	IFT Coil	S74230 yellow	CPU clock	–

SWITCH KNOB

13129101	SDG5P-001	power	100V		(001-215)
13129102	SDG5P-001	power	117V		(001-216)
13129103	SDG5P-502	power	220/240V		(001-217)
13119508	SRM1026	rotary		mode, auto fill in	–
13119806	SRM101C-C	rotary		instrument/track	–
13139129	SLE62301	lever		basic variation	–
13139128	SLP62208	lever		I/F variation	–
13159503	SQPR24-12P	slide		pre-scale	(001-228)
13159105	SSP04205	slide		instrument	(001-293)
13159112	SSF22-07	slide		sync	–
13129901	DS102 #44	push		clear	(001-045)
13129711	KED10001	key		start/stop	–
13129703	KED10903	key		tap	(001-299)
13169601	KHC11901	key		step number	–
2247012700	Knob		N-127		(016-077)
2247012800	Knob		N-128		(016-078)
2247016500	Knob		N-165		–
2247516700	Knob		N-167	white	(016H010)
2247516800	Knob		N-168	orange	(016H012)
2247516900	Knob		N-169	yellow	(016H017)
2247518000	Knob		N-180	red	(016H018)
2247050600	Button		N-506	black power switch	(016-009)

SEMICONDUCTOR

LSI

15179116	μPD650C-085	CMOS CPU	–
15179305	μPD444C or HM4334P-4 (compatible)	CMOS RAM	–

IC

15229802	BA662A	Vari-conductance amp.	–
15159101ZO	MC14001BCP	Quad 2-input NOR gate	–
15159104TO	TC4011BP	Quad 2-input NAND gate	–
15459105TO	TC4013BP	Dual type D flip-flop	–
15159113ZO	MC14051BCP	Analog multi/demultipxr	–
15159303HO	HD14584B	Hex Schmitt trigger	–
15189113	AN6912	Quad comparator	–
15199110TO	TA7179P	±15V Regulator	–
15199106FO	μA7805UC	+5V Regulator	–
15189105	μPC4558C	Dual op amp	–

TRANSISTOR

15119105	2SA733 (P) or (Q)		–
15119113	2SA1015 (GR) or (Y)		–
15119806	2SB596 (O)		–
151291050A	2SC828 (R)	selected noise	–
15129108	2SC945 (P) or (Q)		–
15129121	2SC2021 (R) or (Q), (S)		–
15129815	2SD880 (O)		–
15139101	2SK30ATM (Y)	FET	–
15139103	2SK30ATM (GR)	FET	–

LED

15029103	TLR124	red		–
15029119	SEL2110R	red	S/N up to **10**	–

DIODE

15019120	IS2473	Si diode	–
15019122	IS188FM	Ge diode	–
15019236	W-02	rectifier stack	–
15019209	10E-2		–

POTENTIOMETER

13219310	EVH-LWAD25B52	500Ω (B)	LT, MT, HT tuning	–
13219311	EVH-LWAD25A53	5K (A)	CB level	–
13219312	EVH-LWAD25B14	10K (B)	AC level, SD, snappy	–
13219313	EVH-LWAD25C14	10K (C)	BD tone	–
13219314	EVH-LWAD25B24	20K (B)	CY tone	–
13219315	EVH-LWAD25A15	100K (A)	level	–
13219316	EVH-LWAD25B15	100K (B)	SD tone	–
13219317	EVH-LWAD25B55	500K (B)	BD decay	–
13219318	EVH-LWAD25B26	2M (B)	CY, OH decay	–
13219233	VM10RB10C	50K (A)	master vol.	(028-751)
13219219	VM10RB10C	50K (B)	fine	(028-762)
13219761	GM70EF51E	10K (B)x2	tempo	–
13299114	H1051A013	10K (B) SR19R	trimmer	(030-465)
13299115	H1051A015	22K (B) SR19R	trimmer	(030-467)
13299117	H1051A019	100K (B) SR19R	trimmer	(030-471)
13299119	H1051A021	220K (B) SR19R	trimmer	(030-473)

RESISTOR

15229909	ERSC33G561	560Ω	–

FUSE, FUSE HOLDER

12559104	SGA 0.5A	pri. sec	100/117V	–
12559508	CEE 250mAT	pri. sec	220/240V	–
12199519	Fuse clip TF785			(012-003)

CIRCUIT BOARD ASSEMBLY

7311613006	MAIN BOARD	OP3116-130	(PCB 291-400A)	–
7311614001	VOICING BOARD	VG3116-140	(PCB 291-401A)	–
7311609000	SWITCH BOARD	OP3116-090	(PCB 291-402)	–
7311610000	JACK BOARD (A)	OP3116-100	(PCB 291-403)	–
7311611000	JACK BOARD (B)	OP3116-110	(PCB 291-404)	–
7311605100	POWER SUPPLY BOARD (100/117V)	PS3116-051	(PCB 291-405A)	–
7311605400	POWER SUPPLY BOARD (220/240V)	PS3116-054	(PCB 291-405A)	–

CAPACITOR

13639932JO	SL25VB10BP	10μF 25V	non-polar
13589453MO	ECQ-UC1A473MC 100/117V	0.047μF	polypropylene
13589454MO	ECQ-U2A473MF 220/240V	0.047μF	polypropylene

TERMINAL

13439119	5045-03A		–
13439122	5045-06A		–
13439123	5045-07A		–
13439124	5045-08A		–
13439110	3022-12A		–
13429121	FH1-12S-2.54DS		–
13459101	TT501 D-1 2P	power cord	(042-039)

WIRING ASS'Y

2341021000	N-210	3P	–
2341021100	N-211	3P	–
2341021200	N-212	6P	–
2341021300	N-213	7P	–
2341021400	N-214	7P	–
2341021500	N-215	8P	–

OTHERS

2246010101	Heat sink	N-101		(048-001A)
2215051700	Long nut	N-517 3x8mm		(120-042)
2215050100	Long nut	N-501 3x10mm		(120-001)
2215050200	Long nut	N-502 3x16.4mm		(120-002)
2215050300	Long nut	N-503 3x18mm		(120-003)
2215052400	Boss nut	N-524 3x8mm		(120-052)
2219525600	Holder	N-256	power switch	(064H076)
2219024600	Holder	N-246	main and voicing board	–
2219024700	Holder	N-247	main and voicing board	–
2219024802	Holder	N-248	battery holder	–
2219510600	Holder	N-106	Potentiometer	(064H055)
2219510800	Hplder	N-108	Power cord	(064H074)
2219510900	Holder	N-109	Power cord	(064H075)
12199525	Battery holder	N-525		–
2224011500	Dust cover	N-115	lever switch	(065-261)
2224010200	Dust cover	N-102	slide switch	(065-065)
2202015901	Battery cover	N-159		–
2202016200	Shield cover	N-162	main board	–
2202061201	Protect cover	N-612	top panel	–
2202061701	Protect cover	N-617	top panel	–
2226031000	Cushion	N-310	battery cover	–
2216051100	Fiber spacer	N-511	power cord terminal	–
12369504	Bushing	SR-4N-4		–
12369511	Bushing	BU4801	power cord	–
12369410	Cord fastener	1702B		–

Roland has changed parts codings from 6-digit to 8- or 10-digit.
"N" followed by abridged number should be used in new coding only.
Ex-code is listed at line end for cross reference.